SGS-THOMSON MICROELECTRONICS

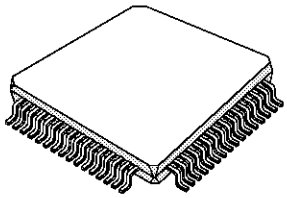
ST75C52

HIGH SPEED FAX MODEM DATA PUMP

- ITU-T V.17, V.29, V.27ter, V.21 WITH FAX SUPPORT
- ITU-T V.23, V.21, BELL 103
- V.17, V.29 (T104), V.27ter SHORT TRAINS
- V.33 HALF-DUPLEX
- 1800Hz OR 1700Hz CARRIER
- SINGLE CHIP COMPLETE DATA PUMP
- SINGLE 5V POWER SUPPLY :
  - TYPICAL ACTIVE POWER CONSUMPTION : 500mW
  - LOW POWER MODE (typ. 5mW)
- EXTENDED MODES OF OPERATIONS :
  - FULL IMPLEMENTATION OF THE V.17, V.33, V.29 AND V.27ter HANDSHAKES
  - AUTODIAL AND AUTOANSWER CAPABILITY
  - PROGRAMMABLE TONE DETECTION AND FSK V.21 FLAG PATTERN DETECTION DURING HIGH SPEED RECEPTION
  - PROGRAMMABLE CALL PROGRESS AND CALL WAITING TONE DETECTORS INCLUDING DTMF
  - PROGRAMMABLE CLASS™ DETECTION CAPABILITY
  - WIDE DYNAMIC RANGE (>48dB)
  - A-LAW VOICE PCM MODE
- VERSATILE INTERFACES :
  - PARALLEL 64 x 8-BIT DUAL PORT RAM
  - SYNCHRONOUS/HDLC PARALLEL DATA HANDLING
  - HDLC FRAMING SUPPORT
  - V.24 INTERFACE
  - FULL OPERATING STATUS REAL TIME MONITORING
  - FULL DIAGNOSTIC CAPABILITY
  - DUAL 8-BIT DAC FOR CONSTELLATION DISPLAY

DESCRIPTION

The SGS-THOMSON Microelectronics ST75C52 chip is a highly integrated modem engine, which can operate with all currently used FAX group III standards up to 14400bps. Full V.21, V.23 and Bell 103 full duplex modem standards are implemented.



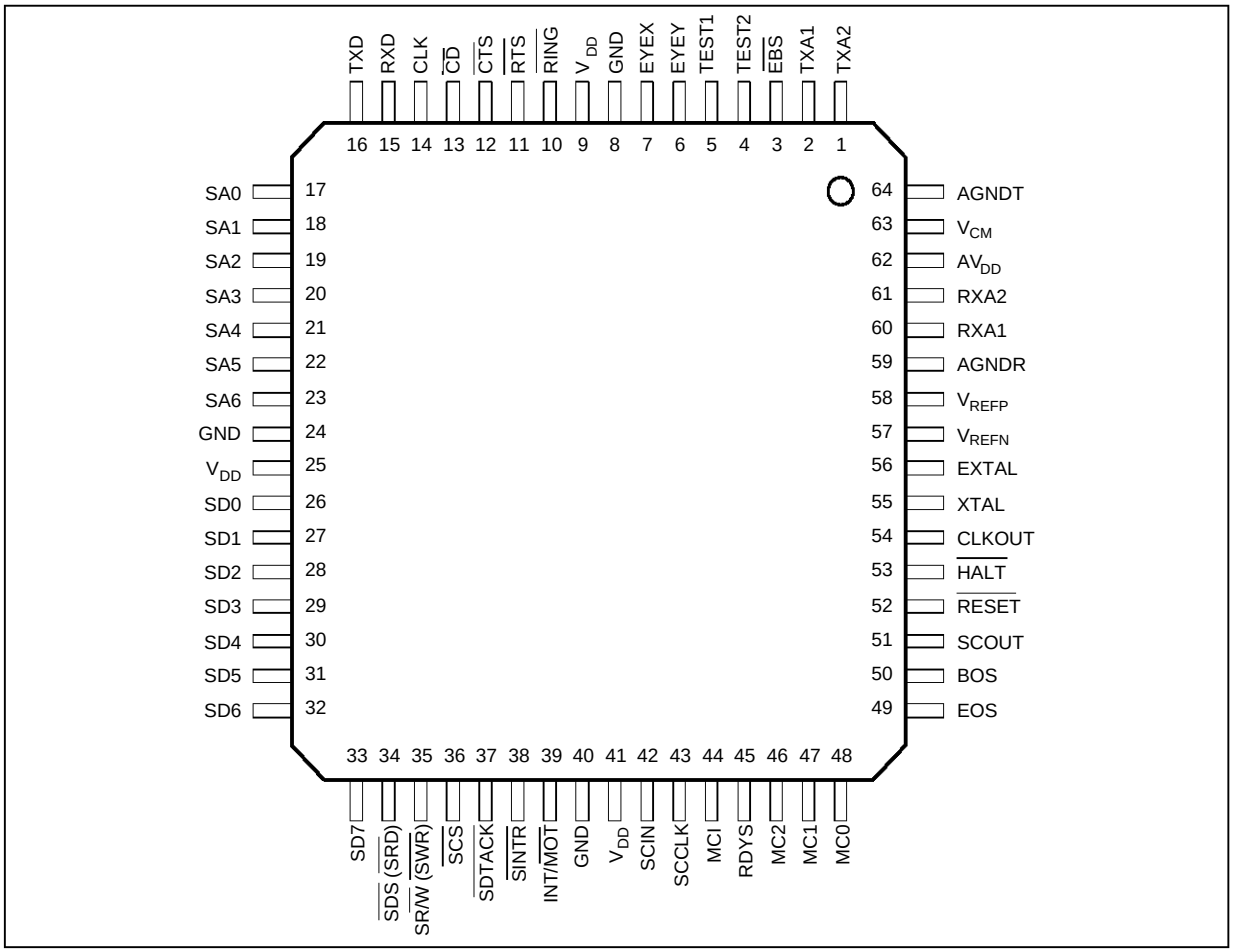
PQFP64
(Plastic Quad Flat Pack)

ORDER CODE : ST75C52 PQFP

SUMMARY

I - PIN DESCRIPTION

I.1 - Pin Connections



I.2 - Host Interface

The exchanges with the control processor proceed through a 64 Bytes DUAL port RAM shared between the ST75C52 and the Host. The signals associated with this interface are :

Pin Name	Type	Description
SD0..SD7	I/O	System Data Bus. 8-bit data bus used for asynchronous exchanges between the ST75C52 and the Host through the dual port RAM. High impedance when exchanges are not active.
SA0..SA6	I	System Address Bus. 7-bit address bus for dual port RAM.
$\overline{SDS}$ ($\overline{SRD}$)	I	System Data Strobe. Active low. Synchronizes all the exchanges. In Motorola mode initiates the exchange, active low. In Intel mode initiates a read exchange, active low.
SR/$\overline{W}$ ($\overline{SWR}$)	I	System Read/Write. In Motorola mode defines the type of exchange read/write. In Intel mode initiates a write exchange, active low.
$\overline{SCS}$	I	System Chip Select. Active low.
$\overline{SDTACK}$	OD	System Bus Data Acknowledge. Active low. Open drain.
$\overline{SINTR}$	OD	System Interrupt Request. Active low. This signal is asserted by the ST75C52 and negated by the host. Open drain.
$\overline{RESET}$	I	Reset. Active low.
$\overline{RING}$	I	Ring Detect Signal : awake ST75C52 from its sleep mode, active low.
INT/$\overline{MOT}$	I	Select Intel/Motorola Interface.

I.3 - Analog Interface

Pin Name	Type	Description
TXA1	O	Transmit Analog Output 1
TXA2	O	Transmit Analog Output 2. Outputs TXA1 and TXA2 provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external continous-time two pole smoothing filter (where $V_{REF} = V_{REFP} - V_{REFN}$).
RXA1	I	Receive Analog Input 1
RXA2	I	Receive Analog Input 2. The analog differential input peak to peak signal must be less than 2 x V_{REF}. It must be preceded by an external continous-time single pole anti-aliasing filter. This filter must be as close as possible to the RXA1 and RXA2 Pins (where $V_{REF} = V_{REFP} - V_{REFN}$).
V_{CM}	I/O	Analog Common Voltage (nominal +2.5V). This input must be decoupled with respect to AGND.
V_{REFN}	I	Analog Negative Reference (nominal V_{CM} - 1.25V). This input must be decoupled with respect to V_{CM}.
V_{REFP}	I	Analog Positive Reference (nominal V_{CM}+1.25V). This input must be decoupled with respect to V_{CM}.

I.4 - V.24 Interface

Pin Name	Type	Description
$\overline{RTS}$	I	Request to Send. Active low.
CLK	O	Data Bit Clock. Falling edge coïncides with DATA change.
$\overline{CTS}$	O	Clear to Send. Active low.
RxD	O	Receive Data
TxD	I	Transmit Data sampled with rising edge of CLK
$\overline{CD}$	O	Carrier Detect. Active low.

I.5 - Miscellaneous

Pin Name	Type	Description
XTAL	O	Internal Oscillator Output. Left open if not used.
EXTAL	I	Internal Oscillator Input, or External Clock
EYEX	O	Constellation X analog coordinate
EYEY	O	Constellation Y analog coordinate
TEST1		To be left open
TEST2		To be left open

Note : The nominal external clock frequency of the ST75C52 is 29.4912MHz with a precision better than $\pm 5.10^{-5}$

I.6 - Boundary Scan Interface

A set of 13 signals are dedicated for Testing the ST75C52 Component. These signals can be used in a development phase, associated with the SGS-THOMSON ST18932 Boundary Scan Development Tools, to Debug the application Hardware and Software. If not used all input signals must be grounded and all output signals left open.

Pin Name	Type	Description
SCIN	I	Scan Data Input
SCCLK	I	Scan Clock
SCOUT	O	Scan Data Output
BOS	I	Begin of Scan Control
EOS	I	End of Scan
MC0..MC2	I	Mode Control
$\overline{HALT}$	I	Stop ST75C52 Execution
MCI	O	Multicycle Instruction
RDYS	O	Ready to Scan Flag
$\overline{EBS}$	I	Enable Boundary Scan. Active low (must be set low in normal mode).
CLKOUT	O	Internal ST75C52 Clock (XTAL frequency divided by 2)

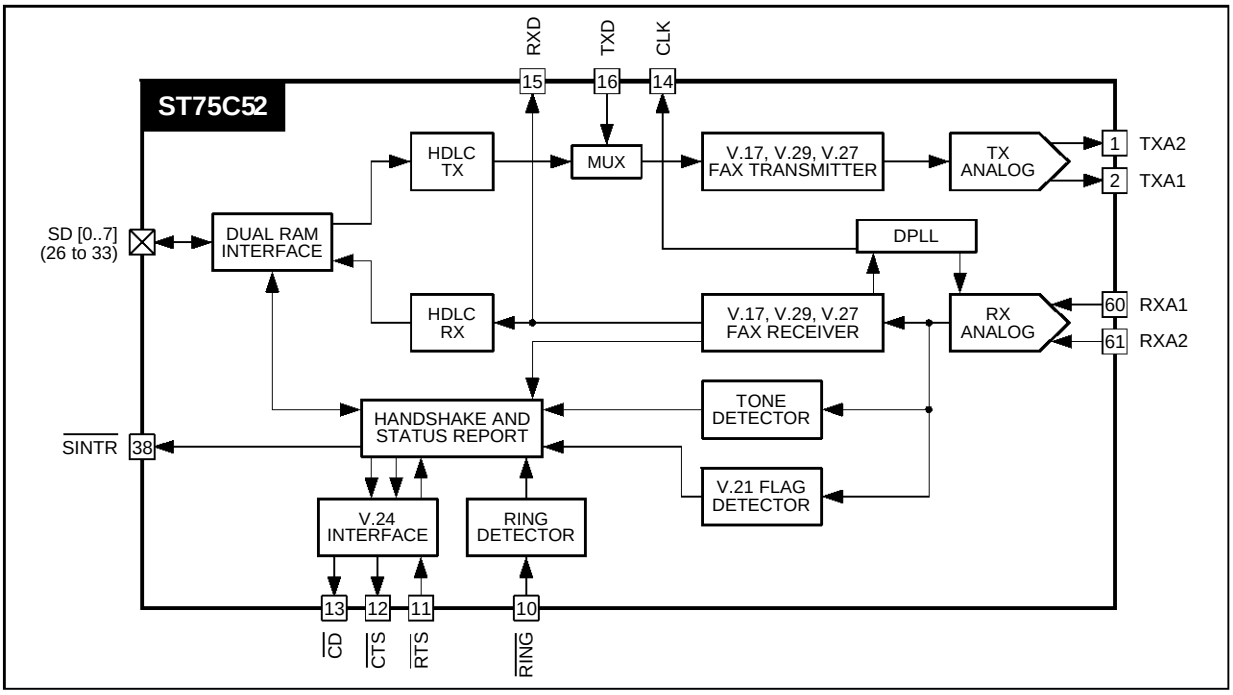
I.7 - Power Supply

Symbol	Parameter
V_{DD}	Digital +5V (Pin 9, 25, 41). To be connected to AV_{DD} (see below).
GND	Digital Ground (Pin 8, 24, 40). To be connected to AGNDT and AGNDR (see below).
AV_{DD}	Analog +5V (Pin 62). To be connected to V_{DD} (see below).
AGNDT	Analog Transmit Ground (Pin 64). To be connected to GND (see below).
AGNDR	Analog Receive Ground (Pin 59). To be connected to GND (see below).

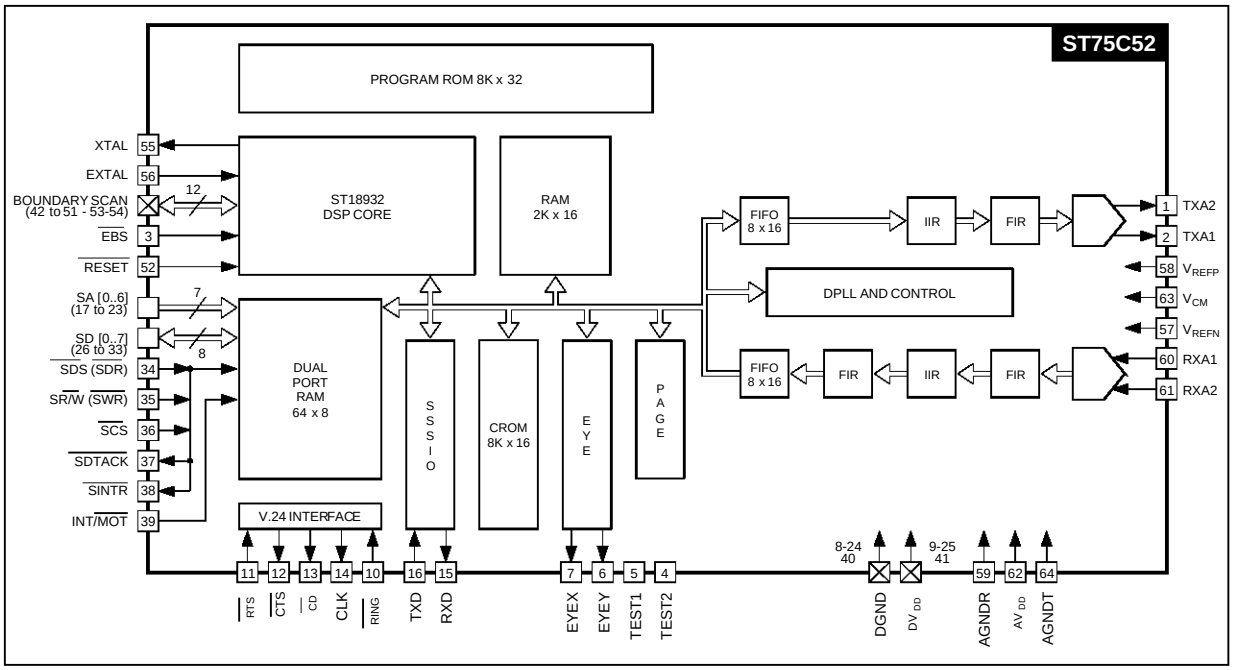
AGNDT and AGNDR must be connected together as close as possible to the chip.
GND and AGNDR board plans should be separated, then connected together as close as possible to the chip, at a single point. Similarly V_{DD} and AV_{DD} must ne connected as close as possible to the chip, at a single point.

II - BLOCK DIAGRAMS

II.1 - Functional Block Diagram



II.2 - Hardware Block Diagram



III - ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical value are given for V_{DD} = +5V and t_{amb} = 25°C.

III.1 - Maximum Ratings (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
V_I, V_{IN}	Digital or Analog Input Voltage	-0.3 to (V_{DD} + 0.3)	V
I_I, I_{IN}	Digital or Analog Input Current	± 1	mA
I_O	Digital Output Current	± 20	mA
I_{OUT}	Analog Output Current	± 10	mA
T_{oper}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature (plastic)	- 40, + 125	°C
P_{tot}	Maximum Power Dissipation	1000	mW

Stresses above those hereby listed may cause damage to the device. The ratings are stress related only and functional operation of the device at conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

III.2 - DC Characteristics

V_{DD} = 5.0V ± 5%, GND = 0V, T_{amb} = 0 to 70°C (unless otherwise specified).

III.2.1 - Power Supply and Common Mode Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current		100	130	mA
I_{DD-lp}	Supply Current in Low Power Mode		1		mA
V_{CM}	Common Mode Voltage	V_{DD}/2 -5%	V_{DD}/2	V_{DD}/2 + 5%	V

III.2.2 - Digital Interface

All digital pins except XTAL Pins.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{IH}	High Level Input Voltage	2.2			V
I_I	Input Current $V_I = V_{DD}$ or V_I = GND	-10	0	+10	µA
V_{OH}	High Level Output Voltage (I_{load} = 2mA)	2.4			V
V_{OL}	Low Level Output Voltage (I_{load} = 2mA)			0.4	V
I_{OZ}	Three State Input Leakage Current (GND < V_O < V_{DD})	-50	0	50	µA
C_{IN}	Input Capacitance		5		pF

Crystal oscillator interface (XTAL, EXTAL).

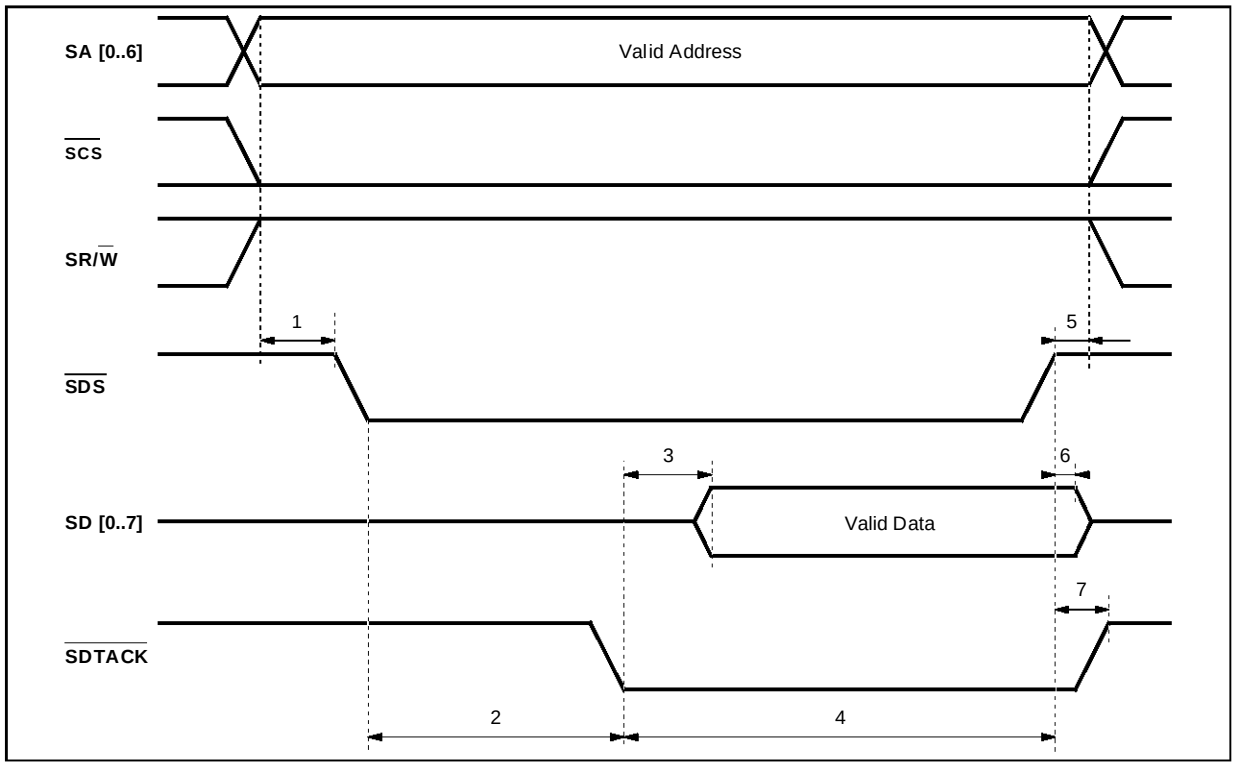
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage			1.5	V
V_{IH}	High Level Input Voltage	3.5			V
I_L	Low Level Input Current GND < V_I < V_{ILmax}	-15			µA
I_H	High Level Input Current VIHmin < V_I < V_{DD}			15	µA

III.2.3 - Analog Interface

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{REF}	Differential Reference Voltage Input = V_{REFP} - V_{REFN}		2.40	2.50	2.60	V
V_{CMOin}	Input Common Mode Offset, v = (RXA1+RXA2)/2 - V_{CM}		-300		300	mV
V_{DIFin}	Differential Input Voltage RXA1 - RXA2				2 x V_{REF}	V_{PP}
V_{CMOout}	Output Common Mode Voltage Offset = (TXA1+TXA2)/2 - V_{CM}		-200		200	mV
V_{DIFout}	Differential Output Voltage TXA1 - TXA2				2 x V_{REF}	V_{PP}
VOFFOut	Differential Output DC Offset (TXA1 - TXA2)		-100		100	mV
Rin	Input Resistance	RXAx	100			kΩ
Rout	Output Resistance	TXAx			20	Ω
RL	Load Resistance	TXAx	10			kΩ
CL	Load Capacitance	TXAx			50	pF

III.3 - AC Electrical Characteristics

III.3.1 - Dual Port RAM Host Read-Cycle Timing (MOTOROLA mode) (1)



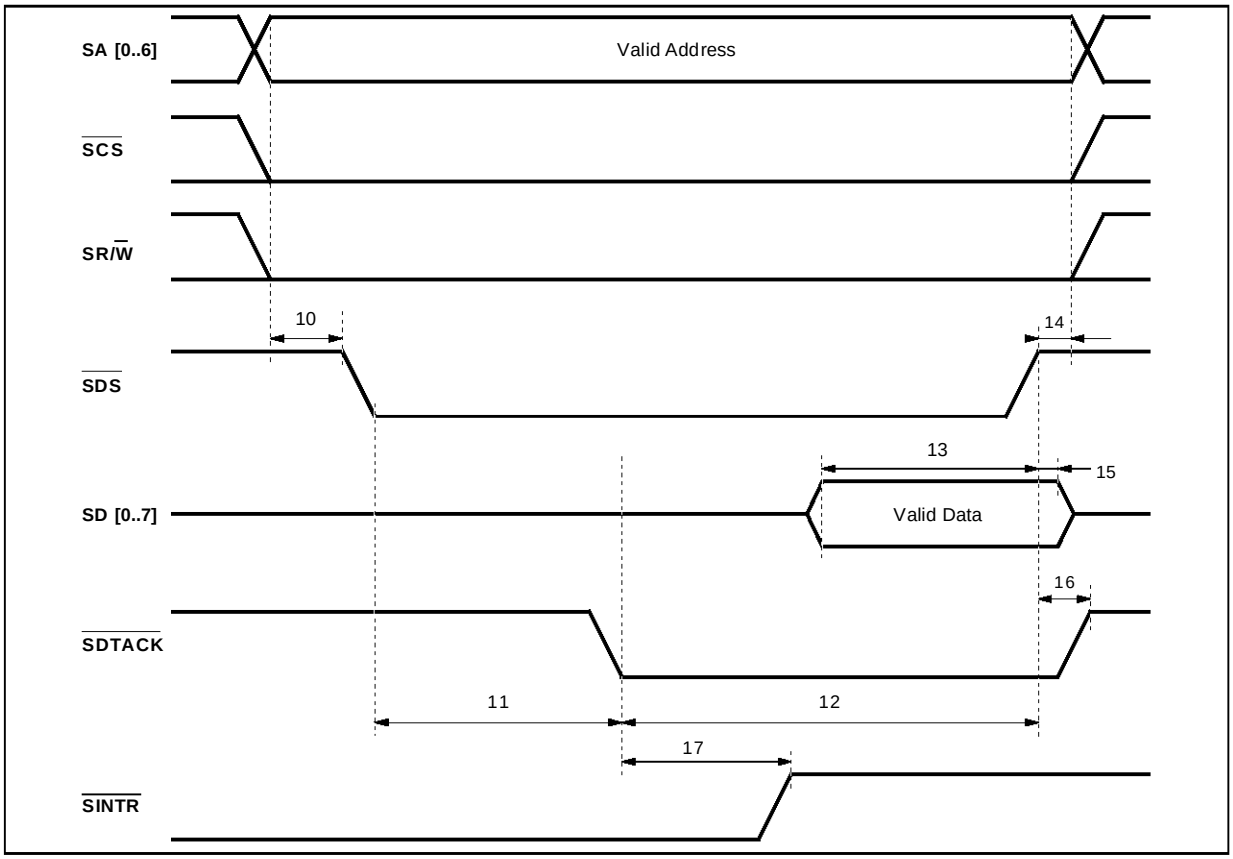
Number	Description	Min.	Typ.	Max.	Unit
1	Address, SR/W, SCS Setup Time	5			ns
2	SDTACK Acknowledge			282(2)	ns
3	SDTACK Prepositionment Time			30	ns
4	Data Strobe Delay	50(3)			ns
5	Address Hold Time	5			ns
6	Data Hold Time	5			ns
7	SDTACK Hold Time	0		10	ns

Notes : 1. This mode is selected if the signal INT/$\overline{MOT}$ is connected to GND.

2. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is $4 \cdot t_c + 10$ ns.

3. If the application does not use the SDTACK signal, the minimum SDS low state must be 340ns (or $5 \cdot t_c$).

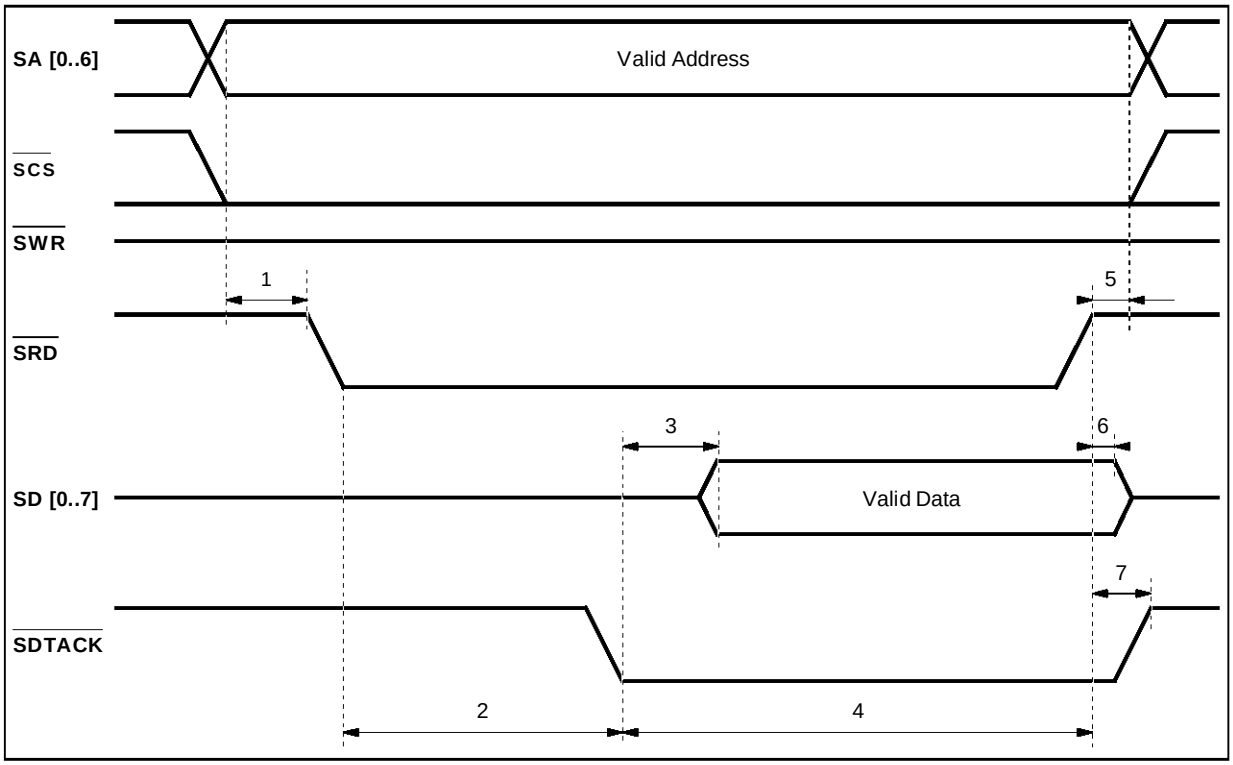
III.3.2 - Dual Port RAM Host Write-Cycle Timing (MOTOROLA mode)



Number	Description	Min.	Max.	Unit
10	Address, SR/W, SCS Setup Time	5		ns
11	SDTACK Acknowledge		282(1)	ns
12	Data Strobe Delay	50(2)		ns
13	Data Setup Time	10		ns
14	Address Hold Time	5		ns
15	Data Hold Time	5		ns
16	SDTACK Hold Time	0	10	ns
17	SINTR Clear Delay	0	78(3)	ns

Notes : 1. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is $4 \cdot t_c + 10$ ns.
2. If the application does not use the SDTACK signal, the minimum SDS low state must be 340ns (or $5 \cdot t_c$).
3. The maximum value is $t_c + 10$ns.

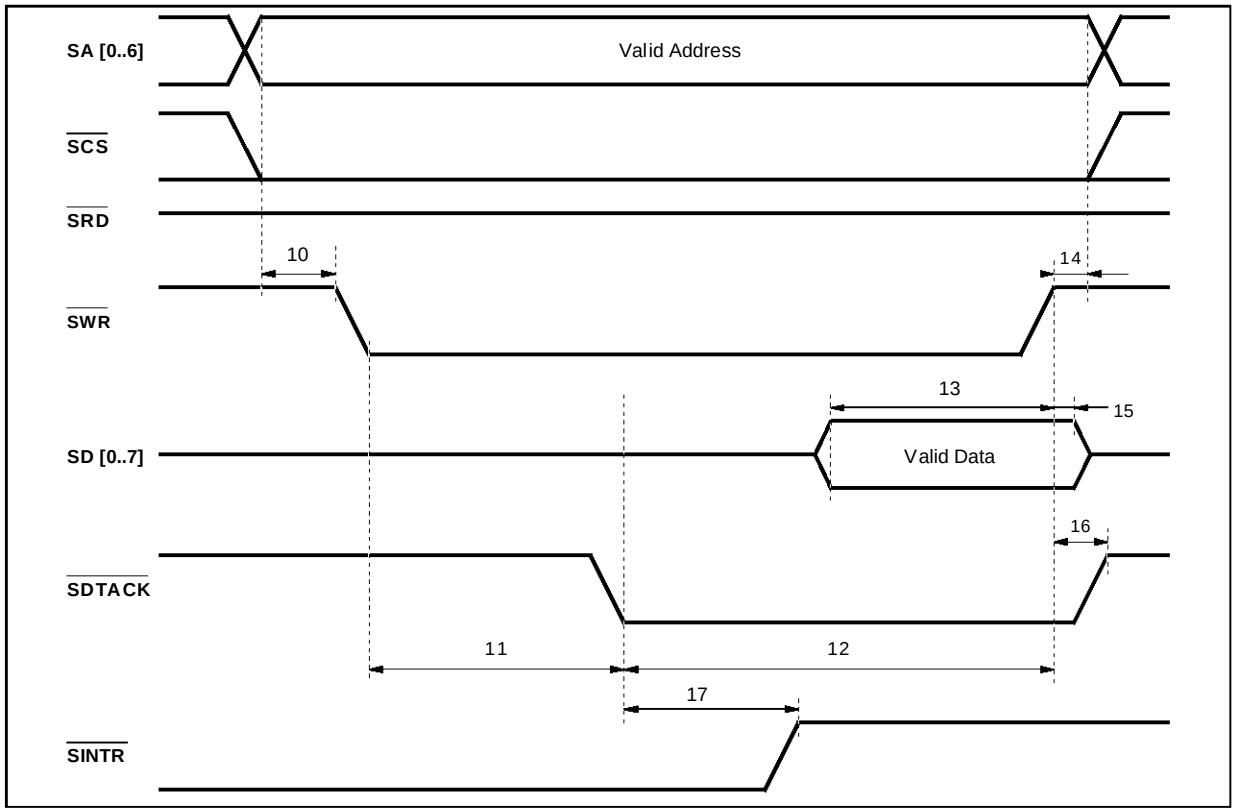
III.3.3 - Dual Port RAM Host Read-Cycle Timing (INTEL mode) (1)



Number	Description	Min.	Typ.	Max.	Unit
1	Address, SCS Setup Time	5			ns
2	SDTACK Acknowledge			282(2)	ns
3	SDTACK Prepositionment Time			30	ns
4	SRD Delay	50(3)			ns
5	Address Hold Time	5			ns
6	Data Hold Time	5			ns
7	SDTACK Hold Time	0		10	ns

Notes : 1. This mode is selected if the signal INT/$\overline{MOT}$ is connected to V_{DD}.
2. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is $4 \cdot t_c + 10$ ns.
3. If the application does not use the SDTACK signal, the minimum SRD low state must be 340ns (or $5 \cdot t_c$).

III.3.4 - Dual Port RAM Host Write-Cycle Timing (INTEL mode)



Number	Description	Min.	Max.	Unit
10	Address, SCS Setup Time	5		ns
11	SDTACK Acknowledge		282(1)	ns
12	SWR Delay	50(2)		ns
13	Data Setup Time	10		ns
14	Address Hold Time	5		ns
15	Data Hold Time	5		ns
16	SDTACK Hold Time	0	10	ns
17	SINTR Clear Delay	0	78(3)	ns

Notes : 1. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is $4 \cdot t_c + 10$ ns.
2. If the application does not use the SDTACK signal, the minimum SWR low state must be 340ns (or $5 \cdot t_c$).
3. The maximum value is $t_c + 10$ns.

IV - FUNCTIONAL DESCRIPTION

IV.1 - System Architecture

The chip allows the design of a complete FAX data-pump without any external component. A versatile dual port RAM allows an easy interface with most micro-controllers.

IV.2 - Operation

IV.2.1 - Modes

The modem implementation is fully compatible with FAX modulation recommendations. The modulation can be either Trellis Coded Modulation (TCM) as in V.17 14400, 12000, 9600, 7200bps rates, Quadrature Amplitude Modulation (QAM) as in V.29 9600, 7200, 4800 and V.27ter 4800 and 2400bps. Other modes of operation include tone and DTMF detection or generation, or speech mode.

IV.2.2 - Transmitter Description

The signal pulses are shaped in a dedicated filter further combined with a compromise transmit equalizer suited for transmission over strongly distorted lines. 3 different compromise equalizers are available and can be selected by software.

IV.2.3 - Receiver Description

The receiver section handles complex signals and uses a fractionally spaced complex equalizer. It is able to cope with distant modem timing drifts up to 10^{-4} as specified in the ITU-T recommendations. It also compensate for frequency drift up to 10Hz and for phase jitter at multiple and simultaneous frequencies.

IV.2.4 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C52. The tones are determined by their frequencies and by the output amplitude level. A set of specific commands are also available for DTMF generation (using two of the four generators available).

IV.2.5 - Tone Detector Description

Sixteen tones can be simultaneously detected by the ST75C52. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR. Detection thresholds are also programmable from -45dBm up to -10dBm. DTMF detection is also available and is performed by a specific filter section (that requires no programming).

IV.2.6 - DTMF Detector Description

A DTMF Detector is included in the ST75C52, it allows detection of valid DTMF Digits. A valid DTMF Digit is defined as a dual Tone with a total power higher than -35dBm, a duration higher than 40ms and a differential amplitude within 8dB (negative or positive).

IV.2.7 - Voice Mode

The ST75C52 voice mode allows the implementation of enhanced telephone functions like answering machines. The incoming samples (9600Hz), received from the line are PCM A-law coded and writen into the dual port RAM. The outpoing samples are decompressed using the same A-law and output to the telephone line.

The voice mode is entered using a CONF command, it can be either transmit voice from the dual RAM Tx buffer to the telephone line, receive voice from the telephone line to the dual RAM buffer, or both of these functions simultaneously. The format of the signal is A-law coded without complementation of the even bits. The buffer mechanism, between the host micro-controler and the ST75C52, is identical to the mechanism used for parallel data exchanges except that it starts immediately after CONF command, the size of the transmit and received buffer, are and must be 8 bytes, there is no need for a XMIT command, and if an overrun or underrun condition occurs no error will be reported to the host processor.

IV.2.8 - Analog Loop Back Test Mode

In any transmission standard and serial data format, the ST75C52 can be configured for analog loop back test.

IV.2.9 - Low Power Mode

Sleep state can be attained by a SLEEP command. Activating the reset signal or any other interrupt signal will wake up the data-pump. When in sleep mode, the dual port RAM is unavailable and the clocks are disabled.

When entering the low power mode, the ST75C52 stops its oscillator, all the peripherals of the DSP core are stopped in order to reduce the power consumption. The dual RAM is made inacessible. The ST75C52 can be awakened by a hardware reset.

When waking up, the ST75C52 processes exactly as after a hardware reset or an INIT command as described after.

There is a maximum time of 20ms to restart the oscillator after waking up and an additional 5ms after the interrupt to be able to accept any command coming from the host.

IV.2.10 - Reset

After a hardware reset, or an INIT command, the ST75C52 clears all its internal memories, clears the whole dual RAM and starts to initialize the delta sigma analog converters. As soon as these initializations are completed, the ST75C52 clears the dual RAM address 0 (COMSYS), generates an interrupt IT6 (command acknoledge) and is programmed to send and receive tones, the bit clock and the sample clock are programmed to 9600Hz. The total duration of the reset sequence is about 5ms. After that time the ST75C52 is ready to execute commands sent by the host micro-controller. The duration of the reset signal should be greater than 700ns.

IV.3 - Modem Interface

IV.3.1 - Analog Interface

The modem designer must provide a proper hybrid interface to the ST75C52. An example of hybrid design is given in paragraphs XII and XIII. The inputs and outputs of the MAFE are differential, achieving thus a better noise immunity. The D/A converter output amplifier includes a single pole low-pass filter, its cut-off frequency is :

F_c - 3dB # 19200Hz.

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components.

IV.3.2 - Host Interface

The host interface is seen by the micro as a 64x8 RAM, with additional registers accessible through an 8-bit address space. A selection Pin (INT/MOT) allows to configure the host bus for either INTEL or MOTOROLA type control signals.

V - USER INTERFACE

V.1 - Dual Port Ram Description

The dual port RAM is the standard interface between the controller and the ST75C52, for either commands or data. This memory is addressed through a 7-bit address bus. The locations from $00 to $3F are RAM locations, while locations from $40 to $50 are control registers dedicated to the interrupt handling.

Several functional areas are defined in the dual port RAM, namely :

- the command area,
- the report area,
- the status area,
- the data buffer area.

V.1.1 - Mapping

V.1.1.1 - Command Area

The command area is located from $00 to $04. Address $00 holds the command byte COMSYS, and the next four locations hold the parameters COMPAR[0..3]. The command parameters must be entered before the command word is issued. Once the command has been entered, the command byte is reset and an acknowledge report is issued. A new command should not be issued before the acknowledge counter COMACK is incremented.

V.1.1.2 - Report Area

The report area is located from address $05 to address $07. Location $05 holds the acknowledge counter COMACK. Each time a command is acknowledged, the report bytes COMREP[0..1] (if any) are written by the ST75C52 into locations $06 and $07, and the content of COMACK is incremented. This counter allows the ST75C52 to accurately monitor the command processing.

V.1.1.3 - Status Area

The status area is located from address $08 to $0A. The error status word SYSERR is located at address $08. This error status word is updated each time an error condition occurs. An optional interruption IT0 may additionally be triggered in the case of an error condition. Locations $09 and $0A hold the general status bytes STATUS[0..1]. The meaning of the bits depends on the mode of operation, and is described in Chapter VII. The third byte at address $0B holds the Quality Monitor byte STAQUA.

V.1.1.4 - Optional Status Area

The user can program (through the DOSR command) the three locations STAOPT[0..2] of the Optional Status Area ($0C to $0E) for the real time monitoring of three arbitrary memory locations.

V.1.1.5 - Data Buffer Area

The data area is made of four 8-byte buffers. Two are dedicated to transmission and the two others to reception. Each of the four buffers is attached to a status byte. the meaning of the status byte depends on the selected format of transmission. Within each buffer, D0 represents the first bit in time.

V.1.2 - Interruptions

The ST75C52 can generate 5 interrupts for the controller. The interrupt handling is made with a set of registers located from $40 to $50.

The interruptions generated by the ST75C52 come from several different sources. Once the ST75C52 raises an interrupt, a signal is sent to the controller. The controller has then to process the interrupt and clear it. The interrupt source can be examined in the Interrupt Source Register ITSRCR located at $50. According to this status byte, the interrupt source can be determined. Then, writing a zero at one of the memory location $40 to $46 (Reset Interrupt Registers ITREST[0..6]) will reset the corresponding interrupt (and thus acknowledge it). These sources of interruptions can be masked globally or individually using the Interrupt Mask Register ITMASK located at $4F.

The interrupt sources are :

- **IT0 : Error/Warning**
  This signifies that an error has occurred and the error code is available in the error status byte SYSERR. This byte can be selectively cleared by the CSE command.
- **IT2 : Tx Buffer**
  Each time the ST75C52 frees a buffer, this interrupt is generated.
- **IT3 : Rx Buffer**
  Each time the ST75C52 has filled a buffer, this interrupt is generated.
- **IT4 : Status Byte**
  This signifies that the status byte has changed and must be checked by the controller.
- **IT6 : Command Acknowledge**
  This signifies that the ST75C52 has read the last command entered by the host, incremented the command counter COMACK, and is ready for a new command.

ITSRCR	X	D6	X	D4	D3	D2	X	D0

D0 = 1 IT0 Pending
D2 = 1 IT2 Pending
Dn = 1 ITn Pending

ITMASK	D7	D6	D5	D4	D3	D2	X	D0

D7 and D0 = 1 IT0 Enable D
D7 and D2 = 1 IT2 Enable D
....
D7 and D6 = 1 IT6 Enable D

V.1.3 - Host Interface Summary

Address (hex)	Description	Size (Byte)	Mnemonic
COMMAND AREA			
$00	Command	1	COMSYS
$01-$04	Command Parameters	4	COMPAR[0..3]
REPORT AREA			
$05	Acknowledge Counter	1	COMACK
$06-$07	Report	2	COMREP[0..1]
STATUS AREA			
$08	Error Status	1	SYSERR
$09-$0A	General Status	2	STATUS[0..1]
$0B	Quality Monitor	1	STAQUA
$0C-$0E	Optional Report	3	STAOPT[0..2]
DATA AREA			
$1C	Data Rx Buffer 0 Status	1	DTRBS0
$1D-$24	Data Rx Buffer 0	8	DTRBF0[0..7]
$25	Data Rx Buffer 1 Status	1	DTRBS1
$26-$2D	Data Rx Buffer 1	8	DTRBF1[0..7]
$2E	Data Tx Buffer 0 Status	1	DTTBS0
$2F-$36	Data Tx Buffer 0	8	DTTBF0[0..7]
$37	Data Tx Buffer 1 Status	1	DTTBS1
$38-$3F	Data Tx Buffer 1	8	DTTBF1[0..7]
INTERRUPT AREA			
$40-$46	Reset Interrupt Reg.	7	ITREST[0..6]
$4F	Interrupt Mask Reg.	1	ITMASK
$50	Interrupt Source Reg.	1	ITSRCR

V.2 - Command Set

The Command Set has the following attractive features :

- user friendly with easy to remember mnemonics,
- possibility of straightforward expansion with new commands to suit specific customer requirements,
- easy upgrade of existing software using previous modem based SGS-THOMSON products.

The command set has been designed to provide the necessary functional control on the ST75C52. Each command is classified according to its syntax and the presence/absence of parameters. In the case of a parametric command, parameters must first be written into the dual port RAM before the command is issued. Acknowledge and error report is issued for each command entered.

V.2.1 - Command Set Summary

V.2.1.1 - Operational Control Commands

INIT Initialize. Initialize the modem engine. Set all parameters to their default values and wait for commands of the control processor. Non parametric command.

IDT Identify. Return the product identification code. Non parametric command.

SLEEP Turn to low power mode, the ST75C52 enters the low power mode and stops its crystal oscillator to reduce power consumption. In this mode all the clocks are stopped and the dual RAM is unreachable. It can be awakened by either a hardware reset, a low level on the RING Pin or a dummy write of its dual RAM.

HSHK Handshake. Begins the handshake sequence. The modem engine generates all the sequences defined in the ITU-T recommendations. A status report indicates to the control processor the state of the handshake. This command only applies to modes where a handshake sequence is defined. A CONF command must have been issued prior to the use of HSHK. Non parametric command.

STOP FAX Stop. Stop FAX Half-duplex transmitter. Non parametric command.

SYNC FAX Synchronize. Start/Stop of FAX Half-duplex receiver. Parametric command.

CSE Clear Status Error. Selectively clears the Error status byte SYSERR. Parametric command.

SETGN Set Gain. This command sets the global gain factor, which is used for the transmit samples. Parametric command.

V.2.1.2 - Data Communication Commands

XMIT Transmit Data. Start/stop the transmission of data in parallel mode. After a XMIT command, the ST75C52 sends the data contained in its dual port RAM.

SERIAL Select Serial or Parallel Mode. This command selects the data source, i.e. either parallel or serial. The parallel mode uses a part of the dual port RAM as a double buffer. The serial mode uses the serial synchronous I/O. Parametric command.

FORM Selects the Transmission Format (only in parallel mode). This command configures the data interface for both receiver and transmitter according to the selected data format. Parametric command (HDLC or synchronous). In serial mode, format is always synchronous.

V.2.1.3 - Memory Handling Commands

MW Memory Write. This command is used to write an arbitrary 16-bit value into the writable memory location currently specified by a parameter. Parametric command.

MR Memory Read. This command allows the controller to read any of the ERAM or CROM (ST75C52 memory spaces) location without interrupting the processor. Parametric command.

CR Complex Read. This command allows the controller to read at the same time the real and imaginary part of a complex value stored in a double ERAM or CROM location. This feature is very interesting for eye pattern software control and for equalization monitoring. This command insures that the real and imaginary parts are sampled in the memory at the same time (integrity). Parametric command.

V.2.1.4 - Configuration Control Commands

CONF Configure. This command configures the modem engine for data transmission and handshake procedures (if any) in any of the supported modes. The transmission parameters are set to their default values and can be modified with the MODC command. Parametric command.

MODC Modify Configuration. This command allows modification of some of the parameters which have been set up by the CONF command. It can also be used to alter the mode of operations (short train). Parametric command.

DOSR Define Optional Status Report. This command allows the modification of the optional status report located in the status area of the dual port RAM. One can thus select a particular parameter to be monitored during all modes of operation. Parametric command.

DSIT Define Status Interrupt. This command allows the programming of the status word bit that will generate an Interrupt to the controller. Parametric command.

V.2.1.5 - Tone Generation Commands

TONE Select Tone. Programs the tone generator(s) for the desired default tone(s). Additional mnemonics provide quick programming of DTMF tones or other currently used tones. Parametric command.

DEFT Define Tone. Programs the tone generator(s) for arbitrary tone synthesis. Parametric command.

TGEN Tone Generator Control. Enables or disables the tone generator(s). Parametric command.

IV.2.1.6 - Tone Detection Commands

TDRC Read Tone Detector Coefficient. Read one Tone Detector Coefficient. Parametric command.

TDWC Write Tone Detector Coefficient. Write one Tone Detector Coefficient. Parametric command.

TDRW Read Tone Detector Wiring. Read one Tone Detector Wiring connection. Parametric command.

TDWW Write Tone Detector Wiring. Write one Tone Detector Wiring connection. Parametric command.

TDZ Clear Tone Detector Cell. Clear internal variables of a Tone Detector Cell. Parametric command.

V.2.1.7 - Miscellaneous Commands

CALL Call a Subroutine. Call a subroutine with one Parameter. Parametric command.

JSR Call a Low Level Subroutine. Call an internal subroutine with one parameter. Parametric command.

V.3 - Command Set Short Form

CCI Command		
Mnemonic	**Value**	**Description**
XMIT	0x01	Transmit Data
SETGN	0x02	Set Transmit Gain
SLEEP	0x03	Power Down the ST75C52
HSHK	0x04	Start Handshake
INIT	0x06	Initialize (Software Master RESET)
SERIAL	0x07	Enable/disable Data Serial Mode
CSE	0x08	Clear Error Status Word
FORM	0x09	Define Parallel Data Format
DOSR	0x0A	Define Optional Status Report
TONE	0x0C	Generate Predefined Tones
TGEN	0x0D	Enable Tone Generator
DEFT	0x0E	Define Arbitrary Tone
MR	0x10	Memory Read
CR	0x11	Complex Read
MW	0x12	Memory Write
DSIT	0x13	Define Status Interrupt
IDT	0x14	Return Product Identification Code
JSR	0x18	Call a Low Level Subroutine
CALL	0x19	Call a Subroutine
TDRC	0x1A	Tone Detector Read Coefficient
TDRW	0x1B	Tone Detector Read Wiring
TDWC	0x1C	Tone Detector Write Coefficient
TDWW	0x1D	Tone Detector Write Wiring
TDZ	0x1E	Tone Detector Clear Cell
CONF	0x20	Configure
MODC	0x21	Modify Default Configuration
STOP	0x25	FAX Stop Transmitter
SYNC	0x26	FAX Synchronize Receiver

V.4 - Status - Reports

V.4.1 - Status

The ST75C52 has a dedicated status reporting area located in its dual port RAM. This allow a continuous monitoring of the status variables without interrupting the ST75C52.
The first status byte gives the error status. Issuing of an error status can also be flagged by a maskable interrupt for the controller. The signification of the error codes are given in Chapter VII.
The second and third status bytes give the general status of the modem. These status include for example the ITU-T circuit status and other items described in appendix. These two status can generate, when a change occurs, an interrupt to the controller ; each bit of the two byte word can be masked independently.
The forth byte gives in real time a measure of the reception quality. This information may be used by the controller to monitor the quality of the received bits.
Three other locations are dedicated for custom status reporting. The controller can program the ST75C52 for a real time monitoring of any of its internal RAM location. High byte or low byte of any word can thus be monitored.

V.4.2 - Reports

The ST75C52 features an acknowledge and report facility. The acknowledge of a command is monitored by a counter COMACK located in the dual port RAM. Each time a command is read from the command area, the ST75C52 will increment this counter. For instance, when a MR (Memory Read) command is issued, the data is first written in the report area, and the counter is incremented afterwards. This way of processing insures data integrity and gives additional synchronization between the controller and the data pump.

V.5 - Data Exchanges

The ST75C52 accepts many kinds of data exchange : the default mode uses the synchronous serial exchange. Other modes include HDLC framing support and synchronous parallel exchanges. Detailed description of the Data Buffer Exchanges modes is available in the paragraph IX.

V.5.1 - Synchronous Parallel Mode

The data exchanges are made through the dual port RAM and are byte synchronous oriented. The double buffer facilities of the ST75C52 allow an efficient buffering of the data.

V.5.1.1 - Transmit

The controller must first fill at least the first buffer of data (Tx Buffer 0) with the bits to be transmitted. In order to perform this operation, the controller must first check the Tx Buffer 0 status word DTTBS0. If this buffer is empty, the controller fills the data buffer locations (up to 64 bits), and then writes in DTTBS0 the number of bytes contained in the buffer. The controller can then either proceed with the second buffer or initiate the transmission with a XMIT command.
The ST75C52 copies the contents of the data buffer and then clears the buffer status word in order to make it again available, then generates an IT2 interrupt. The number of bytes specified by the status word is then queued for transmission. The process goes on with the two buffers until an XMIT command stops the transmission. After the finishing XMIT command has been issued, the last buffers are emptied by the ST75C52.
Errors occur when both buffers are empty while the transmit bit queue is also empty. Error is signalled with an IT0 interruption to the controller.

V.5.1.2 - Receive

The controller should take care of releasing the Rx buffers before the Data Carrier Detect goes true. This is made by writing zero in the Rx Buffer Status 0 and 1. The ST75C52 then fills the first buffer, and once filled sets the status word with the number of bytes received and then generates an IT3 interrupt. It then takes control of the second buffer and operates the same way. The controller must check the status of the buffers and empty them. Once the data read, the controller must release the used buffer and wait for the next buffer to be filled.
Error occurs when both buffers are declared full, and incoming bits continue to arrive from the line. Error is signaled by an IT0 interrupt.

V.5.2 - HDLC Parallel Mode

This mode implements part of the High Level Data Link Control formats and procedures. It is well suited for error correcting protocols like ECM or FAX T4/T30 recommendations. It supports the flagging generation, 16-bit Frame Check Sequence, as well as the Zero insertion/deletion mechanism.

V.5.3 - Serial Exchanges

The other mode of operation for data exchanges is the Serial Synchronous Mode. In this mode, the data I/O is made through the V.24 interface (page 4). Even when using the parallel mode described above, the received bits are available on the ST75C52 RxD Pin. See paragraph VII.2.1 table for clock values.

VI - COMMAND SET DESCRIPTION

The appendix A contains the description of the complete command set. Commands are presented according to the following form :

COMMAND — Command Name Meaning — COMMAND

Opcode Hexadecimal digit

X	X	X	X	X	X	X	X

Synopsis Short description of the functions performed by the command.

Parameters

Field	Byte	Pos.	Value	Definition
Name	X	b..a	xx *	Explanation of the parameter Default value

Field — Name of the addressed bit field.

Byte — Index (or address in the dual port RAM) of the parameter byte (from 1 to 4).

Pos. — Bit field position inside the parameter byte. Can either be a single position (from 0 to 7, 0 being LSB) or a range.

Value — Possible values for the bit (resp. bit field). Range means all values are allowed. A star means a default value. Values are expressed either under the form of a bit string, or under hexadecimal format.

CALL — Call a Subroutine — CALL

Opcode: 19

0	0	0	1	1	0	0	1

Synopsis CALL allows to execute a part of the ST75C52 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

CONF — Configure for Operations — CONF

Opcode 20

0	0	1	0	0	0	0	0

Synopsis CONF allows the complete definition of the ST75C52 operation, including the mode of operation (tone, FAX transmit, FAX receive, voice transmit, voice receive, DTMF receive, ...) and the modem parameters (standard, speed, ...).

Parameters

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	-	Mode of operation, see below
CONF_ANAL	1	4	0 1	Normal mode Analog loop back (test mode only)
CONF_PSTN	1	5	0 1	PSTN (carrier detect set to -43/-48dBm) Leased line (carrier detect -33/-38dBm)
CONF_AO	1	6	0 1	Answer mode (FSK full duplex only) Originate mode (FSK full duplex only)
CONF_V24	1	7	0 1	Do not use RTS pin signal Use RTS pin signal
CONF_MODE	2	5..0	1 3 4 7 8 9 C D Other	Bell 103 (full duplex) V.21 (full duplex) V.23 (full duplex) V.27ter V.29 V.17 V.33 (half duplex) V.21 channel 2 Reserved
CONF_TXEQ	2	7..6	0 1 2 3	No transmit equalizer Transmit equalizer #1 Transmit equalizer #2 Transmit equalizer #3
CONF_CAR	3	0	0 1	1800Hz carrier (V.17/V.33 only) 1700Hz carrier (V.17/V.33 only)
CONF_SP0	3	7..5	xx1 x1x 1xx	2400bps allowed (V.27) 4800bps allowed (V.27, V.29) 7200bps allowed (V.29, V.17)
CONF_SP1	4	2..0	xx1 x1x 1xx	9600bps allowed (V.29, V.17) 12000bps allowed (V.17, V.33) 14400bps allowed (V.17, V.33)

According with the 4 first bits of the CONF_OPER the ST75C52 is put into the following mode of operation.

CONF_OPER	Transmit	Received
0000*	Tones	Tones
0010	Voice	Tones
0100	Tone	DTMF
0110	Voice	DTMF
1000	Tones	Voice
1010	Voice	Voice
1111	Modem	Modem
Other	Not allowed	Not allowed

CR — Complex Read — CR

Opcode: 11

0	0	0	1	0	0	0	1

Synopsis CR allows the reading of a complex parameter. The parameter specifies the parameter address (for the real part : the imaginary part is next location). CR returns the high byte value of both real and imaginary part of the addressed complex parameter.

Parameters

Field	Byte	Pos.	Value	Definition
CR_ADDR_L	1	7..0		Low byte of the 16-bit address
CR_ADDR_H	2	7..0		High byte of the 16-bit address

CSE — Clear Error Status — CSE

Opcode: 08

0	0	0	0	1	0	0	0

Synopsis CSE is used to clear the ST75C52 error status SYSERR byte. It is also used as an acknowledge to the error condition handler. For details, please refer to the corresponding appendix.

Parameters

Field	Byte	Pos.	Value	Definition
ERR_MASK	1	7..0		Error mask See report appendix for detailed meaning

DEFT — Define Arbitrary Tone — DEFT

Opcode: 0E

0	0	0	0	1	1	1	0

Synopsis DEFT programs one of the four tone generator for arbitrary tone generation. The parameter is the frequency of the generated tone expressed in Hertz between 0 and 3600Hz.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_GEN_SL	1	1..0		Index of the tone generator (3..0)
TONE_FREQ_L	2	7..0		Low byte of the frequency
TONE_FREQ_H	3	7..0		High byte of the frequency (internally masked with 0F)
TONE_SCALE	4	7..0		Amplitude scaling factor (high byte) 3F gives the nominal amplitude

DOSR — Define Optional Status Report — DOSR

Opcode: 0A

0	0	0	0	1	0	1	0

Synopsis DOSR specifies the address of the RAM variables to be monitored in the 3 locations STAOPT[0..2] of the dual port RAM. It also specifies the assignment within the 3 locations.

Parameters

Field	Byte	Pos.	Value	Definition
STA_OPT_ASS	1	1..0	0..2	Index of the STAOPT destination
STA_OPT_ADL	2	7..0		Low byte of source address
STA_OPT_ADH	3	3..0		High byte of source address
STA_OPT_HL	3	7	0 1	Select low byte of source Select high byte of source

DSIT — Define Status Interrupt — DSIT

Opcode: 13

0	0	0	1	0	0	1	1

Synopsis DSIT specifies the bit mask used with the STATUS[0] and STATUS[1] byte to generate an interrupt IT4 to controller. Each time a bit change happens in the status words, assuming the corresponding bit mask will be set, an interrupt will be generated.

Parameters

Field	Byte	Pos.	Value	Definition
STA_IT_MSK0	1	7..0		Status[0] bit mask pattern
STA_IT_MSK1	2	7..0		Status[1] bit mask pattern

Notes : The default IT Status is 0x3F for STATUS[0] and 0xFF for STATUS[1].

FORM — Select Transmission Format — FORM

Opcode: 09

0	0	0	0	1	0	0	1

Synopsis FORM defines the type of transmission used. This format is valid only in the parallel data mode. The default format, unless specified, is synchronous.

Parameters

Field	Byte	Pos.	Value	Definition
X_SYNC	1	1..0	00* 01 10 11	Synchronous format Transmit continous "1" (1) HDLC framing Transmit continous "0" (1)

Notes : 1. This format is only valid for the transmiter.

HSHK — Handshake — HSHK

Opcode: 04

0	0	0	0	0	1	0	0

Synopsis HSHK is used to command the ST75C52 to begin the transmit handshake sequence processing. The progress of the handshake is reported to the control processor.

Parameter Non parametric command.

IDT — Identify — IDT

Opcode: 14

0	0	0	1	0	1	0	0

Synopsis IDT Return the ST75C52 Hardware and Software release number. See paragraph VII.1.4.

Parameter Non parametric command.

INIT — Initialization — INIT

Opcode: 06

0	0	0	0	0	1	1	0

Synopsis INIT forces the ST75C52 to reset all parameters to their default conditions and restart operations.

Parameter Non parametric command.

Notes : This command makes a software reset of the ST75C52 and so cannot have the regular handshake protocol. It does not increment the COMACK, neither generate an Interrupt.

JSR — Call a Low Level Subroutine — JSR

Opcode: 18

0	0	0	1	1	0	0	0

Synopsis JSR allows to execute a part of the ST75C52 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

MODC — Modify Configuration — MODC

Opcode: 21

0	0	1	0	0	0	0	1

Synopsis MODC allows modification of the configuration for special purpose. This command has no effect while in data mode, the parameters are just sampled when starting to transmit or receive. The value of these parameters are not affected when sending a CONF command.

Parameters

Field	Byte	Pos.	Value	Definition
MODC_SH	1	6	0* 1	Normal training sequence Short training (1) sequence
MODC_FPT	2	3..2	00* 01 10	No echo protection tone Long echo protection tone (180ms) Short echo protection tone (30ms)

Notes : 1. Short train sequence must be preceded by at least one normal training sequence.

MR — Memory Read — MR

Opcode: 10

0	0	0	1	0	0	0	0

Synopsis MR allows the reading of a 16-bit parameter. The parameter specifies the parameter address.

Parameters

Field	Byte	Pos.	Value	Definition
MR_ADDR_L	1	7..0		Low byte of the 16-bit address
MR_ADDR_H	2	7..0		High byte of the 16-bit address

MW — Memory Write — MW

Opcode: 12

0	0	0	1	0	0	1	0

Synopsis MW allows the writing of a 16-bit parameter. The parameter specifies the address as well as the value to be transferred.

Parameters

Field	Byte	Pos.	Value	Definition
MW_ADDR_L	1	7..0		Low byte of the 16-bit address
MW_ADDR_H	2	7..0		High byte of the 16-bit address
MW_VALUE_L	3	7..0		Low byte of the 16-bit value
MW_VALUE_H	4	7..0		High byte of the 16-bit value

SERIAL — Select Serial or Parallel Mode — SERIAL

Opcode: 07

0	0	0	0	0	1	1	1

Synopsis SERIAL defines the data path, i.e. either serial or parallel.

Parameters

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0* 1	Use serial link for Tx Data Use parallel link for Tx Data
RX_SDATA	1	1	0* 1	Use only serial link for Rx Data Use also parallel link for Rx Data

Notes : The received Bits always go to the output pin RXD, even when the RX_SDATA bit is set.

SETGN — Set Output Gain — SETGN

Opcode: 02

0	0	0	0	0	0	1	0

Synopsis SETGN is a command which sets the scaling factor of the transmit samples. It is used for setting the output level or for setting the level of the tone generators. The gain value is given in the form of a 2's complement 16-bit value.

Parameters

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-bit gain value
GAIN_H	2	7..0	range 7F*	High byte of the 16-bit gain value

Example

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	-5	47FA	-10	287A
-1	7214	-6	4026	-11	2413
-2	65AC	-7	392C	-12	2026
-3	5A9D	-8	32F5	-13	1CA7
-4	50C3	-9	2D6A	-14	198A

SLEEP — Turn to Sleep Mode — SLEEP

Opcode: 03

0	0	0	0	0	0	1	1

Synopsis SLEEP is used to force the ST75C52 to turn to low power mode.

Parameter Non parametric command.

Notes : When receiving this command the ST75C52 will stop processing and so cannot have the regular handshake protocol. It does not increment the COMACK, neither generate an Interrupt. A negative level on the RING Pin or a dummy dual RAM write will awake the ST75C52, generate an IT5 Interrupt and execute a Software Reset (idem **init**).

STOP — FAX Stop Transmitter — STOP

Opcode: 25

0	0	1	0	0	1	0	1

Synopsis STOP is used, in FAX Modes, to force the ST75C52 to turn off the transmitter in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27recommendation.

Parameter Non parametric command.

Notes : When receiving this command the ST75C52 will stop sending regular Data. In parallel mode this command must be preceded by a **XMIT** Stop command. In parallel mode the ST75C52 will wait until all the transmit buffers are sent before starting the Stop sequence.

SYNC — FAX Synchronize the Receiver — SYNC

Opcode: 26

0	0	1	0	0	1	1	0

Synopsis SYNC is used, in FAX Modes, to force the ST75C52 to Start/Stop the receiver in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27 recommendation. As soon as the ST75C52 receives the **SYNC** Start command it sets its receiver to detect the FAX synchronization signal. This command is the equivalent **HSHK** command for the receiver.

Parameters

Field	Byte	Pos.	Value	Definition
RX_SYNC	1	0	0* 1	Stop receiver Start receiver synchronization

TDRC — Tone Detector Read Coefficient — TDRC

Opcode: 1A

0	0	0	1	1	0	1	0

Synopsis TDRC Read one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 Other	Biquad coefficient Energy coefficient Static level Reserved

The command answer is : Low Byte of Coefficient followed by High Byte of Coefficient.

TDRW — Tone Detector Read Wiring — TDRW

Opcode: 1B

0	0	0	1	1	0	1	1

Synopsis TDRC Read Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

The command answer is:

a) If TD_W_ADDR = 0 :
- First Byte is the Node Number of the Signal connected to Biquadratic Filter input.
- Second Byte is the Node Number of the Signal connected to the Energy estimator input.

b) if TD_W_ADDR = 1 :
- First Byte is the Node Number of the Signal connected to Comparator Negative input.
- Second Byte is the Node Number of the Signal connected to the Comparator Positive input.

TDWC — Tone Detector Write Coefficient — TDWC

Opcode: 1C

0	0	0	1	1	1	0	0

Synopsis TDWC Write one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 Other	Biquad coefficient Energy coefficient Static level Reserved
TD_COEFL	3	7..0		Low byte of coefficient
TD_COEFH	4	7..0		High byte of coefficient

TDWW — Tone Detector Write Wiring — TDWW

Opcode: 1D

0	0	0	1	1	1	0	1

Synopsis TDRC Write Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

If TD_W_ADDR = 0 (Select Biquad and Energy Inputs)

Parameters

Field	Byte	Pos.	Value	Definition
TD_W_ERN	3		0..3F	Energy estimator signal input
TD_W_BIQ	4		0..3F	Biquad filter signal input

If TD_W_ADDR = 1 (Select Comparator Inputs)

Parameters

Field	Byte	Pos.	Value	Definition
TD_W_CN	3		0..3F	Negative comparator signal input
TD_W_CP	4		0..3F	Positive comparator signal input

TDZ — Tone Detector Clear Cell — TDZ

Opcode: 1E

0	0	0	1	1	1	1	0

Synopsis TDZ Clears all internal variables of one Tone detector cell including Filter local variables and energy estimator. This command must be sent after changing coefficients of a cell to avoid instability.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number

TGEN — Enable/disable Tone Generators — TGEN

Opcode: 0D

0	0	0	0	1	1	0	1

Synopsis TGEN causes the ST75C52 to enable or disable the four tone generators.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_0_ENA	1	0	0* 1	Generator #0 disabled Generator #0 enabled
TONE_1_ENA	1	1	0* 1	Generator #1 disabled Generator #1 enabled
TONE_2_ENA	1	2	0* 1	Generator #2 disabled Generator #2 enabled
TONE_3_ENA	1	3	0* 1	Generator #3 disabled Generator #3 enabled

TONE — Predefined Tones — TONE

Opcode: 0C

0	0	0	0	1	1	0	0

Synopsis TONE programs the tone generators for the predefined tones. The tone generators #0 and eventually #1 are reprogrammed with this command. Eventually the tone generator #0 and #1 are enabled. Using a value not in the following table will disable tone generator #0 and #1.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_SELECT	1	5..0	0 1 2 3 4 5 6 7 8 9 A B C D E F 10 11 12 13	DTMF 0 (941 & 1336Hz) DTMF 1 (697 & 1209Hz) DTMF 2 (697 & 1336Hz) DTMF 3 (697 & 1477Hz) DTMF 4 (770 & 1209Hz) DTMF 5 (770 & 1336Hz) DTMF 6 (770 & 1477Hz) DTMF 7 (852 & 1209Hz) DTMF 8 (852 & 1336Hz) DTMF 9 (852 & 1477Hz) DTMF A (697 & 1633Hz) DTMF B (770 & 1633Hz) DTMF C (852 & 1633Hz) DTMF D (941 & 1633Hz) DTMF * (941 & 1209Hz) DTMF # (941 & 1477Hz) Answer tone (2100Hz) Tone (1650Hz) Answer tone (2225Hz) Tone (1300Hz)

XMIT — Start/stop Transmission — XMIT

Opcode: 01

0	0	0	0	0	0	0	1

Synopsis XMIT start or stop the transmission of the Parallel Transmit Data. This command work only if the Parallel Transmit Data mode has been selected with a **SERIAL** command.

Parameters

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0* 1	Stop transmission Start transmission

VII - STATUS DESCRIPTION

This appendix is dedicated to the ST75C52 reporting features. in the following sections the command acknowledge process and the report and status definitions are explained.

VII.1 - Command Acknowledge and Report

VII.1.1 - Command Acknowledge Process

(see Figure 1)

The ST75C52 features an acknowledge process based on a counter COMACK. On power-on reset (or INIT command), this counter's value is set to 0. Each time a command is successfully executed by the ST75C52, the acknowledge counter COMACK is incremented. This allows a precise monitoring of the command entered and avoids command collision.

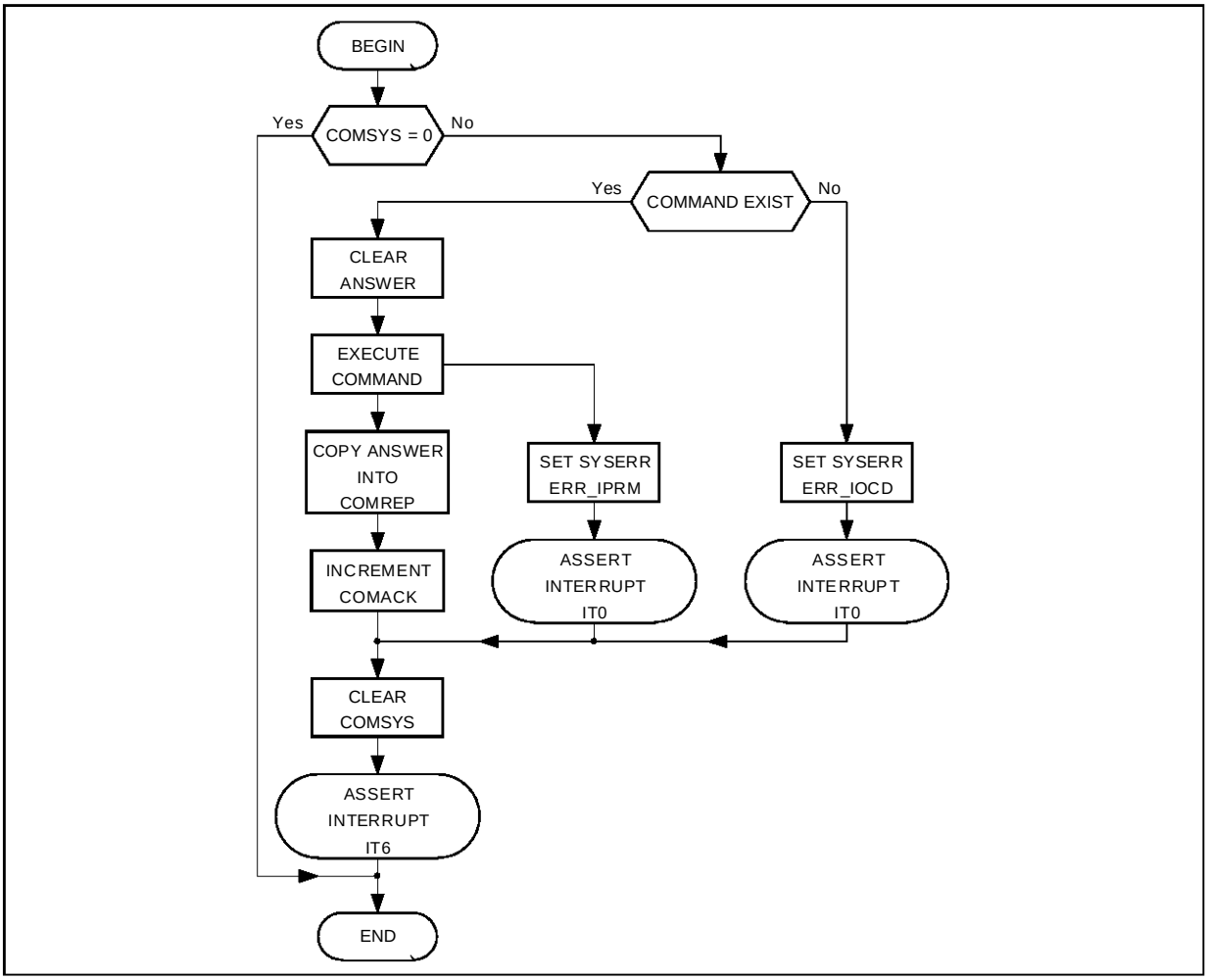
In the case of a memory reading command (CR, TDRC, TDRW, IDT or MR) once the command entered is executed, the report area is filled and the acknowledge counter is incremented afterwards. This insures that the controller will read the value corresponding to its request.

Furthermore, the ST75C52 resets the value of the COMSYS register once the command has been read. The interruption IT6 is raised just after the counter is incremented.

VII.1.2 - Reports Specification

The report section of the Dual Port RAM is dedicated to memory reading. In response to a CR, MR, TDRC, TDRW, IDT commands, the value read is transferred to the report registers COMREP[0..1].

Figure 1 : Command Acknowledge Process



VII.1.3 - CR Command

Issuing a CR command causes the ST75C52 to dump a specific memory location in complex mode. This instruction is particularly useful for equalizer state analysis or for software eye-pattern display. The report area has this meaning :

RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0	COMREP[0]
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	COMREP[1]

RP0..RP7 is the MSB part of the 16-bit value of the real part and IP0..IP7 is the MSB part of the imaginary part. The CR command insures that the real and imaginary part of the desired complex value are sampled internally at the same time. The address given in the parameter field of CR is the address of the real part.

VII.1.4 - MR/TDRC/TDRW/IDT Commands

The report issued by the MR/TDRC/TDRW/IDT commands follow the same rules as for CR. The report meaning is :

D7	D6	D5	D4	D3	D2	D1	D0	COMREP[0]
D15	D14	D13	D12	D11	D10	D9	D8	COMREP[1]

D0..D15 is the 16-bit value required by the MR/TDRC command.

In the case of IDT, D15..D12 contains the product identification (2 for ST75C52), D11..D8 contains the hardware revision identification and D7..D0 contains the software revision identification.

VII.2 - Modem Status

VII.2.1 - Modem Status Description

The Status of ST75C52 is divided into 4 fields :

- The error status byte SYSERR that provides information about error. This status can trigger an IT0 interrupt,
- The general status byte STATUS[0] and STATUS[1] that contains all the modem signals. These status bytes can trigger an IT4 interrupt,
- The quality status STAQUA, that contains the quality of the received transmission,
- The optional status bytes STAOP[0], STAOP[1] and STAOP[2], that contains additional information regarding the ST75C52 operating mode. This default information can be changed to monitor any internal variables using the DOSR command.

All these informations are updated on a Baud basis :

Mode	Baud Rate (2) (Hz)	CLK (Hz)
Tone, DTMF, Voice	2400	9600
Bell 103 (full duplex)	2400	9600
V.21 (full duplex)	2400	9600
V.23 (full duplex)	2400	9600
V.27ter 2400bps	1200	2400
V.27ter 4800bps	1600 (1)	4800
V.29	2400	9600/7200/4800
V.17	2400	14400/12000/9600/7200
V.33	2400	14400/12000
V.21 channel 2	2400	300

Notes : 1. The tone detectors outputs are update 800 times by second.

2. This baud rate defines also, the maximum command rate. Each baud time the ST75C52 looks at the COMSYS location (addesss $00) to see if a command have been sent by the host processor. If the content of this location is different from zero the ST75C52 execute the command.

Starting at the adddress $08 the status area have the following format :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$08	SYSERR	ERR_RTK	-	-	ERR_IPRM	ERR_IOCD	-	ERR_RX	ERR_TX
$09	STATUS0	STA_109F	STA_CPT10	STA_CPT1	STA_CPT0	STA_RING	STA_106	STA_107	STA_109
$0A	STATUS1	STA_DTMF	STA_FLAG	-	STA_HR	STA_AT	STA_CCITT	-	STA_H
$0B	STAQUA	-	Quality						
$0C	STAOP0	Depend on operating mode (see below)							
$0D	STAOP1								
$0E	STAOP2								

VII.2.2 - Error Status

The error status changes each time an error occurs. When the ST75C52 signals an error by setting one of the SYSERR bit, it generates an interrupt IT0. These bits can only be cleared by the host controler using the CSE command.

The meaning of the different bits of the SYSERR byte is discribed below :

SYSERR		
Field	**Pos.**	**Meaning when set**
ERR_TX	0	Transmit buffer underflow. Loss of synchronisation between the host and ST75C52 transmit data buffer managment.
ERR_RX	1	Receive buffer overflow. Loss of synchronisation between the host and ST75C52 receive data buffer managment.
ERR_IOCD	3	Incorrect CCI command
ERR_IPRM	4	Incorrect parameter for the CCI command
ERR_RTK	7	Real time kernel error. ST75C52 not able to perform all its tasks within the baud period (transmit or receive samples lost).

VII.2.3 - Modem General Status

The modem general status word is composed of two bytes STATUS[0] and STATUS[1]. Any bit change can generate an IT4 interrupt. Using the DSIT command allows the selection of the corresponding bit that will generate an interrupt each time they will change. The default pattern is $3F for STATUS[0] and $FF for STATUS[1].

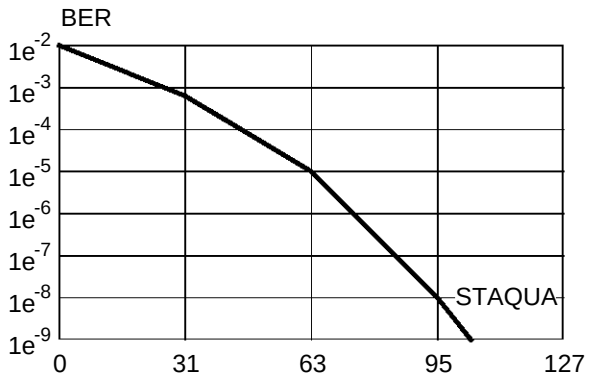
The different bits have the following meaning :

STATUS[0]		
Field	**Pos.**	**Meaning when set**
STA_109	0	CCITT circuit 109 (carrier detect). Indicates that valid data are received. When 0 the output data RxD are clamped to constant mark. Valid only in modem mode.
STA_107	1	CCITT circuit 107 (data set ready). Valid only in modem mode.
STA_106	2	CCITT circuit 106 (clear to send). Indicates that the training sequence has been completed and that any data at TxD pin (serial mode) or in the transmit buffer (parallel mode) will be transmitted. valid only in modem mode.
STA_RING	3	Ring detected. A ring signal (from 15Hz to 68Hz) is present at the RING pin. Valid only in tones modes. The precise frequency can be read in the optional status byte STAOP2. The detection time is 1 period of the ring signal. The detection lost time in 20ms after the last transition on the ring signal.
STA_CPT0	4	Call progress tone detector #0. Low pass filter 650Hz. Valid only in tones modes.
STA_CPT1	5	Call progress tone detector #1. High pass filter 600Hz. Valid only in tones modes.
STA_CPT10	6	Signal in filter #0 is highter than #1. Valid only in tones modes.
STA_109F	7	Fast Carrier Detect. Valid only in modem mode.

STATUS[1]		
Field	**Pos.**	**Meaning**
STA_H	0	Transmit synchronisation in progress. Valid only in modem mode.
STA_CCITT	2	CCITT 2100Hz versus 2225Hz answer tone detect. Valid if STA_AT is set. Valid only in tones modes.
STA_AT	3	Answer tone (either 2100Hz or 2225Hz) detected. Valid only in tones modes.
STA_HR	4	Receive synchronisation in progress. Valid only in modem mode.
STA_FLAG	6	V.21 channel 2 flag detect. Valid only in FAX modem mode and tone mode.
STA_DTMF	7	DTMF digit detect. The digit itself is available in the optional status byte STAOP2. Valid only in DTMF receive mode.

VII.2.4 - Quality Status

The quality byte STAQUA monitors an evaluation of the line quality. It is updated once per baud and its value ranges from 127 (perfect quality) to 0 (terrible quality). This value is automaticaly adjusted according to the current receiving mode. Refer to the following chart to convert the value into its Bit Error Rate equivalence.



75C52-22.EPS

VII.2.5 - Optional Status

According to the operating mode of the ST75C52 the optional status is displaying different informations.

The optional status are automatically reprogrammed after each CONF command with the address of the variables to monitor according with the operating mode selected (CONF_OPER). After the CONF command the user must overwrite this default programming by using the DOSR command.

VII.2.6 - Default Optional Status in Tone Mode

While in tone mode the format of the STAOP word is as follows :

Add.	**Name**	**Bit**							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0C	STAOP0	TDT7	TDT6	TDT5	TDT4	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15	TDT14	TDT13	TDT12	TDT11	TDT10	TDT9	TDT8
$0E	STAOP2	RING_PERIOD (1)							

Notes : 1. RING_PERIOD is valid when the bit 3 of the STATUS[0] (STA_RING) goes high. This value is updated at each falling edge of the RING signal. The RING_PERIOD value must be divided by 2400 to obtain the period in seconds.

2. TDTx is the output of the tone detector x.

VII.2.7 - Default Optional Status in DTMF Receiver Mode

While in DTMF receiver mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7 (1)	TDT6 (1)	TDT5 (1)	TDT4 (1)	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15 (1)	TDT14 (1)	TDT13 (1)	TDT12 (1)	TDT11 (1)	TDT10 (1)	TDT9 (1)	TDT8 (1)
$0E	STAOP2	DTMF_DIGIT (2)							

Notes : 1. These cells are used by the DTMF detector.
2. DTMF_DIGIT is valid when the bit 7 of STATUS[1] (STA_DTMF) goes high. This value remains unchanged until a new DTMF digit is detected.

VII.2.8 - Default Optional Status in Modem Mode

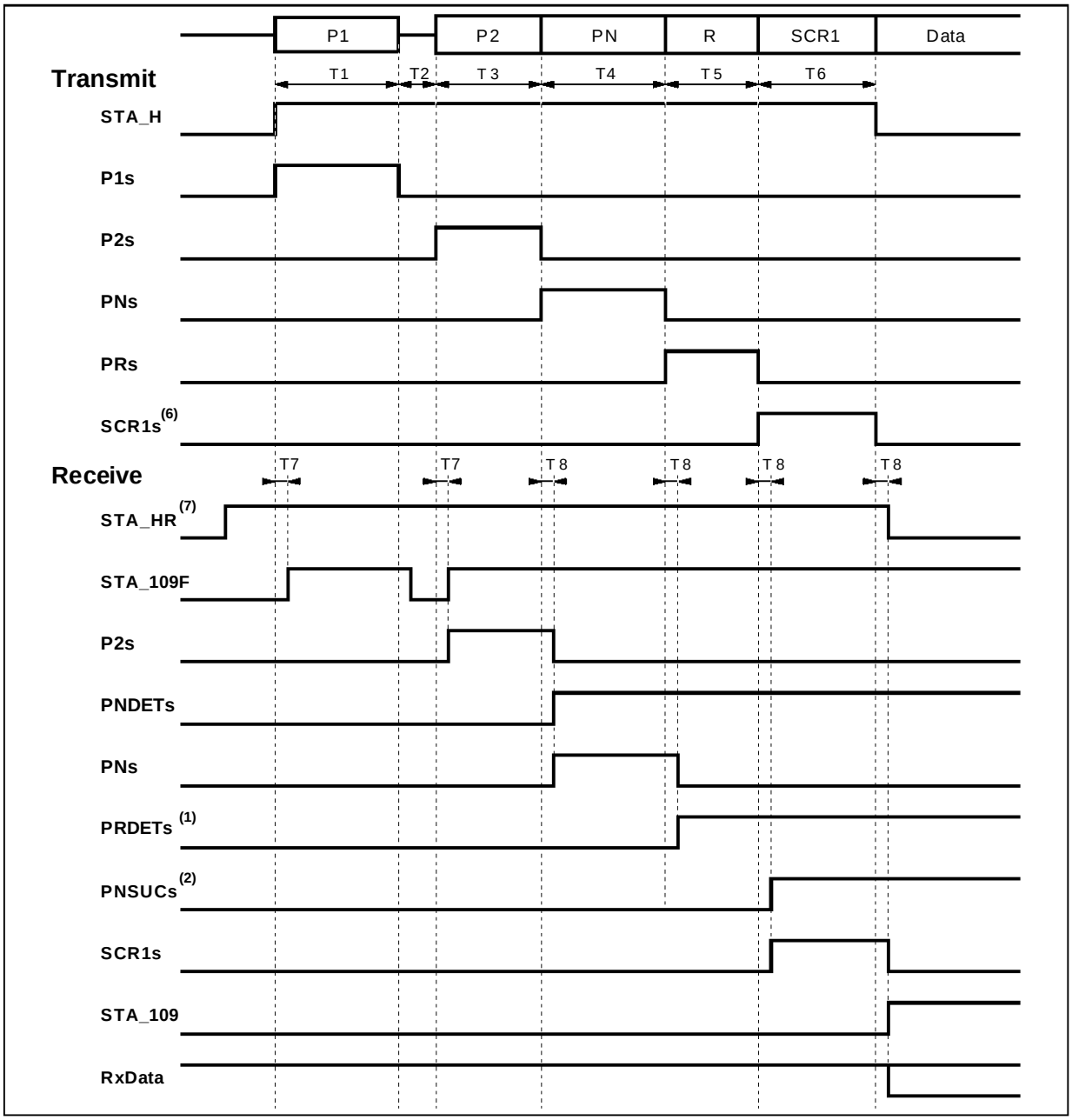
While in modem mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	x	x	x	SPEED (2)				SPVAL (1)
$0D	STAOP1	Not used							
$0E	STAOP2	PNSUCs	PRDETs	PNDETs	SCR1s	PRs	PNs	P2s	P1s

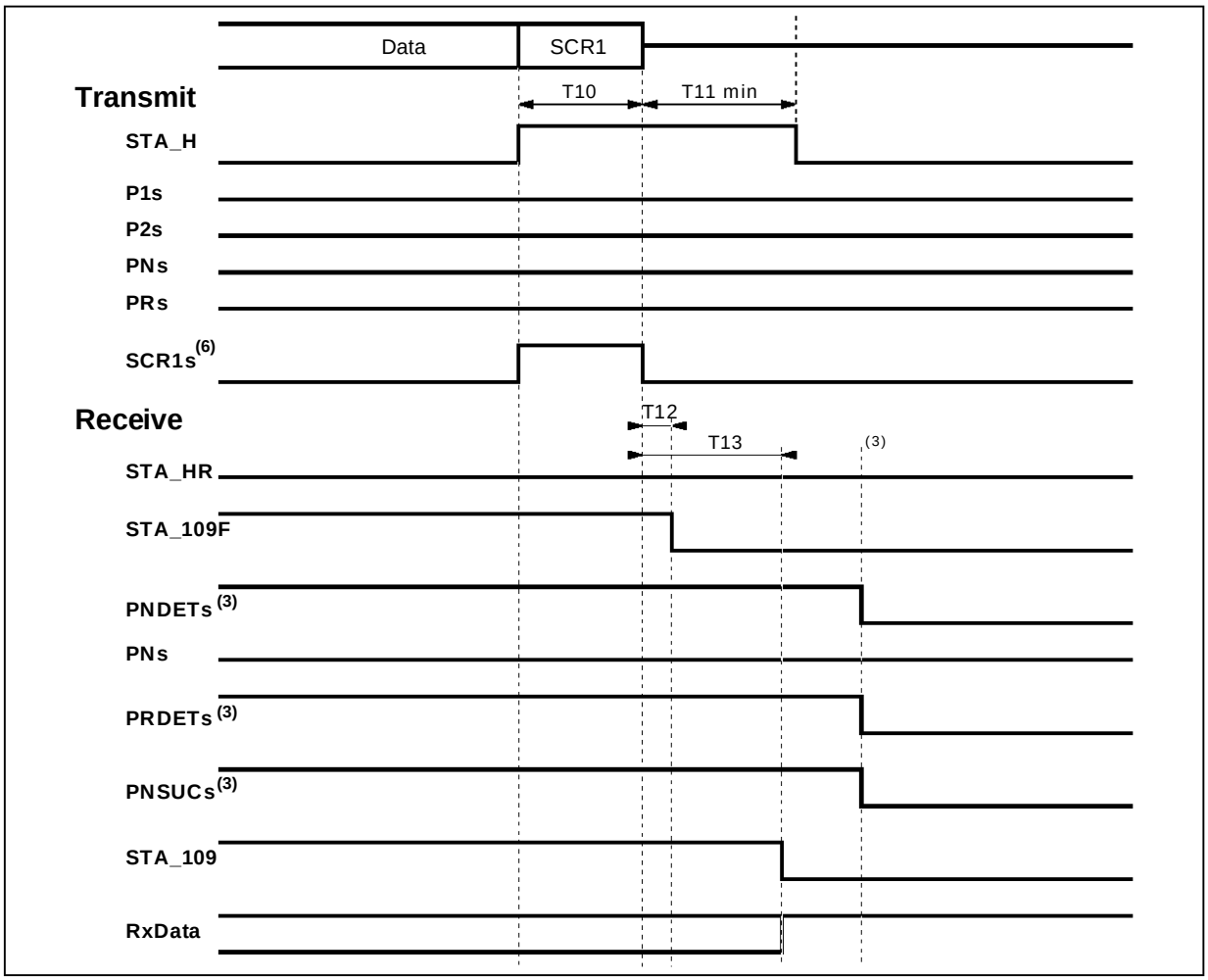
Notes : 1. SPVAL is active in V.33 receiver only at the same time as the rising transition of the SCR1s signal. Went SPVAL is set, it indicates that the SPEED bits contain the data speed information.
2. SPEED is valid in V.33 receiver only. It can have 2 values, after the SCR1s signal goes high : 1000 for 14400bps and 0111 for 12000bps.
3. The STAOP2 bit reflects the progression of the synchronization. The STAOP2 bits have the following meaning :

Name	Position	Description	Tx	Rx
P1s	0	Unmodulated carrier sequence. Optional, used for echo protection.	X	
P2s	1	Continuous 180° phase reversal sequence	X	X
PNs	2	Equalizer trainning sequence	X	X
PRs	3	V.33 and V.17 rate sequence	X	
SCR1s	4	Continuous scrambled 1 sequence	X	X
PNDETs	5	Turned on after PN sequence detection		X
PRDETs	6	Turned on after PR sequence detection (V.33 and V.17 only)		X
PNSUCs	7	Turned on after succesfull training of the receive equalizer. When on at the end of the synchronization, the transmition BER is statisticaly bellow 10ppm.		X

With the following timing :



Mode	T1 (4)	T1p (5)	T2	T3	T4	T5	T6	T7	T8	Unit
V.17	192	30	22	107	1240	27	20	5	7	ms
V.17 short	192	30	22	107	16	0	20	5	7	ms
V.29	192	30	22	53	160	0	20	5	7	ms
V.29 short	192	30	22	41	26	0	8	5	7	ms
V.27 4800	192	30	22	31	670	0	5	5	7	ms
V.27 4800 short	192	30	22	9	36	0	5	5	7	ms
V.27 2400	192	30	22	42	895	0	7	6	7	ms
V.27 2400 short	192	30	22	12	48	0	7	6	7	ms



Mode	T10	T11	T12	T13	Unit
V.17	13	20	8	25	ms
V.17 short	13	20	8	25	ms
V.29	13	20	8	25	ms
V.29 short	13	20	8	25	ms
V.27 4800	20	30	8	25	ms
V.27 4800 short	20	30	8	25	ms
V.27 2400	27	40	8	25	ms
V.27 2400 short	27	40	8	25	ms

Notes : 1. In the case of V.29 or V.27, PRs and PRDETs bits are not active.
2. PNSUCs indicates the quality of the Rx signal that will give a ber of approximation of $1e^{-5}$.
3. After sending the command SYNC0, all bits are reset.
4. When using long echo protection tone, otherwise 0.
5. When using short echo protection tone, otherwise 0.
6. STA-106 is set at the end of T6 and reset at the beginning of T10.
7. After sending the command SYNC1, this bit is set.

VIII - TONE DETECTORS

VIII.1 - Overview

The general purpose TS75C52 tone detectors block is a powerful module that covers a lot of applications :

- call progress tone detection, fully programmable for all countries,
- DTMF detection,
- FAX, voice, data automatic detection,
- call waiting detection, while in voice or data mode.

VIII.2 - Description

The tone detector block is a set of 16 identical Cells. Each cell is composed of a Double Biquadratic Filter, a Power estimator section, a Static level and a Level comparator.

Each Biquadratic Filter, Power Estimator and Static Level can be programmed using a complete set of Commands (**TDRC**, **TDRW**, **TDWC**, **TDWW**, **TDZ**).

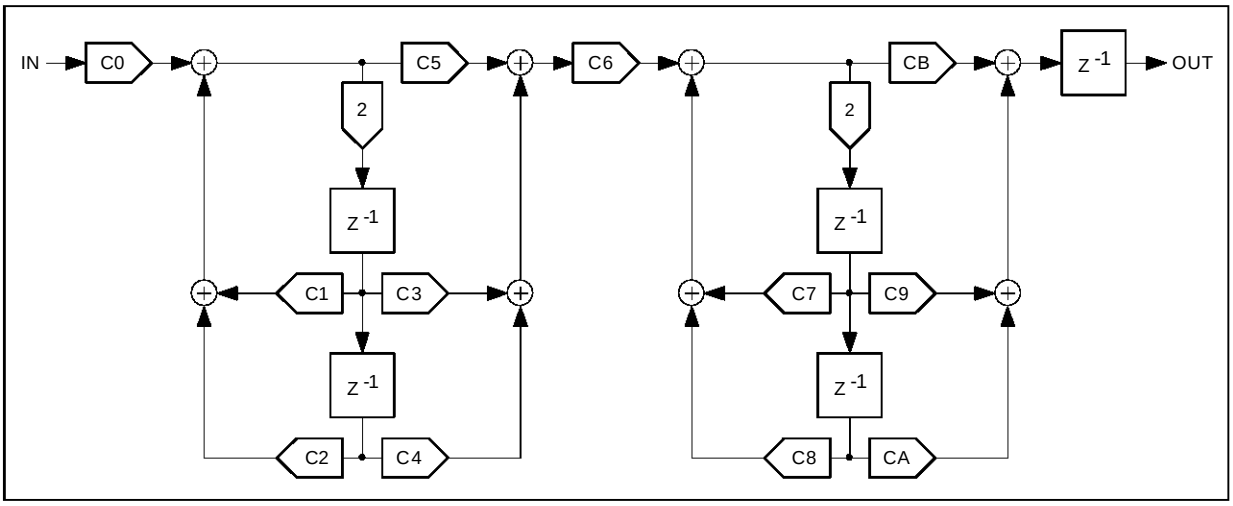
The wiring between the different Cells can be defined by the user, using the associatedCommand allowing a wide range of applications.

The 16 Comparator Outputs give, on a baud basis, the information into two 8 bits words **TONEDET0** (for cells number 0 to 7) and **TONEDET1** (for cells number 8 to F). These TONEDET variables can be accessed using a **MR** command or, more easily, monitored on a baud basis using the **DOSR** command.

VIII.2.1 - Biquadratic Filters

Each Biquadratic Filter is a double regular section that can perform any Transfer function with 4 Poles and 4 Zeros. This routine is run on a sample basis.

Figure 2 : Biquadratic IIR Filter



The corresponding transfer function is :

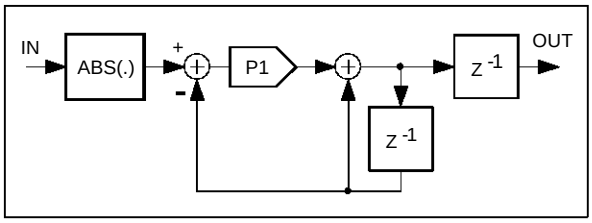
$$\frac{Out}{Input} = C0 \cdot \frac{C5 + 2 \cdot C3 \cdot z^{\pm 1} + 2 \cdot C4 \cdot z^{\pm 2}}{1 \pm 2 \cdot C1 \cdot z^{\pm 1} \pm 2 \cdot C2 \cdot z^{\pm 2}} \cdot C6 \cdot \frac{CB + 2 \cdot C9 \cdot z^{\pm 1} + 2 \cdot CA \cdot z^{\pm 2}}{1 \pm 2 \cdot C7 \cdot z^{\pm 1} \pm 2 \cdot C8 \cdot z^{\pm 2}} \cdot z^{\pm 1}$$

Note : All coefficients are coded on 16 bits 2's complement in the range +1, -1 (Q15). To avoid the possibility of overflow the user must check that the internal node must not be higher that 0.5 (in Q15 representation).

VIII.2.2 - Power Estimation

The Power estimation Cell is needed to measure the amplitude of the different tones. It is run on a sample basis.

Figure 3 : Power Estimator



The corresponding transfer function is :

$$Out = \left| Input \right| \cdot z^{\pm 1} \cdot \frac{P1}{1 \pm (1 \pm P1) \cdot z^{\pm 1}}$$

VIII.2.3 - Static Level

A single Threshold level is associated with each Cell. It can be use to compare the output of a Power Estimation with an Absolute Value.

VIII.2.4 - Comparator

The Comparator computes, on a baud basis, the difference of the signal on its Positive and Negative Inputs. If the result is Higher that zero it sets the corresponding bit into the TONEDET[0..1] word; if not it clear this bit.

VIII.2.5 - Wiring

The user must specify the connection (wiring) between the input/output of the Filter, the input/output of the Power estimator, the output of the static levels and the two inputs of the Comparators.

The output signals have an absolute address:

Node Address		
Signal Name	**Address**	**Description**
Ground	00	Signal always equal to 0000
RxSig	01	Receive signal from the Analog front end
RxSig2	02	Receive signal multiplied by 2
RxSig4	03	Receive signal multiplied by 4
	04..0F	Reserved
Filter[0..F]	10..1F	Biquadratic Filter Outputs
Power[0..F]	20..2F	Power Estimator Outputs
Level[0..F]	30..3F	Static Levels

The user will specify the inputs of the filters, Power and Comparator. At least one input must come from the RxSig (node 01, 02 or 03). It is mandatory to connect all unused cell inputs to the Ground signal (node 00).

Figure 4 : Tone Detector Wiring Address (first half)

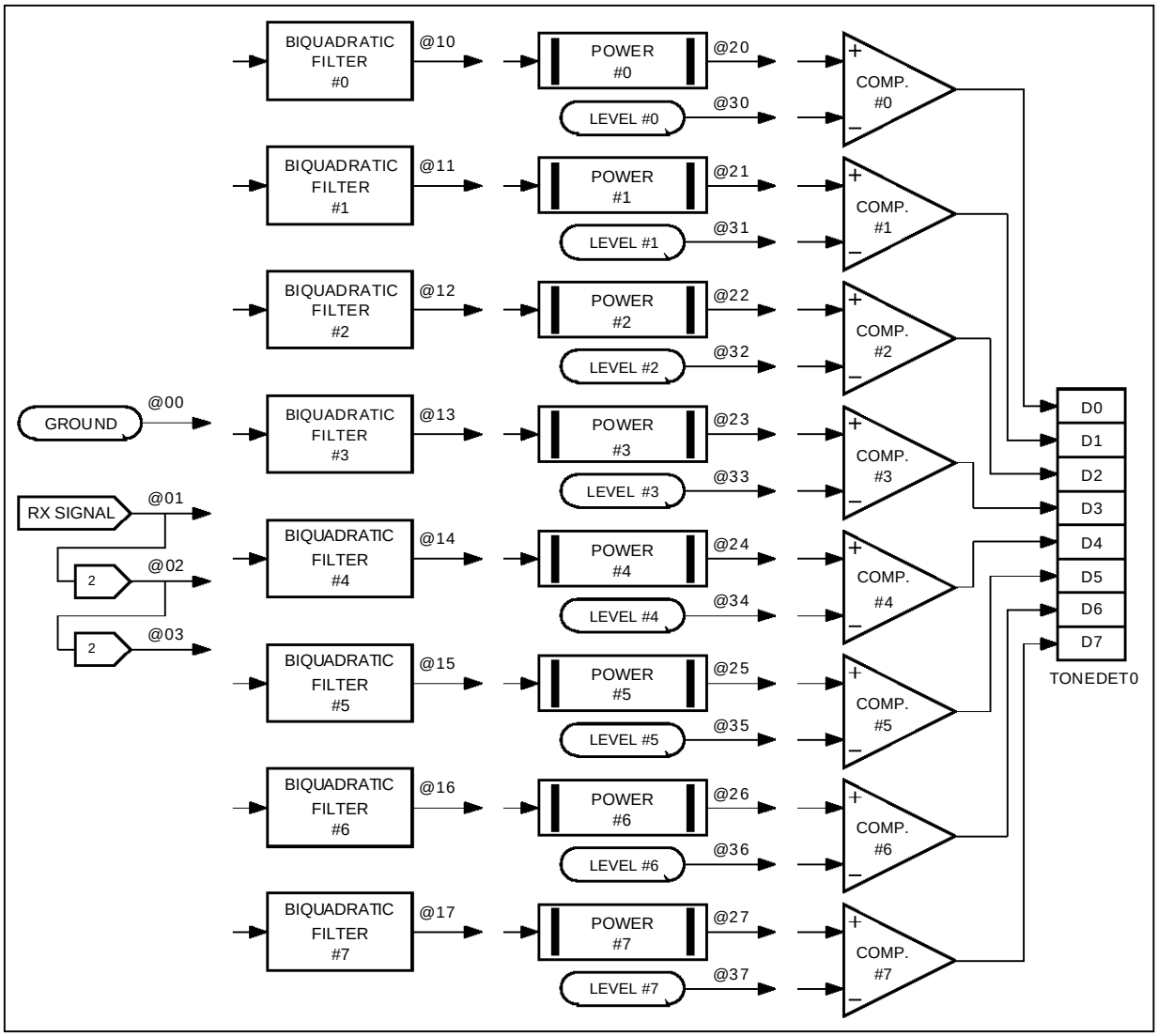
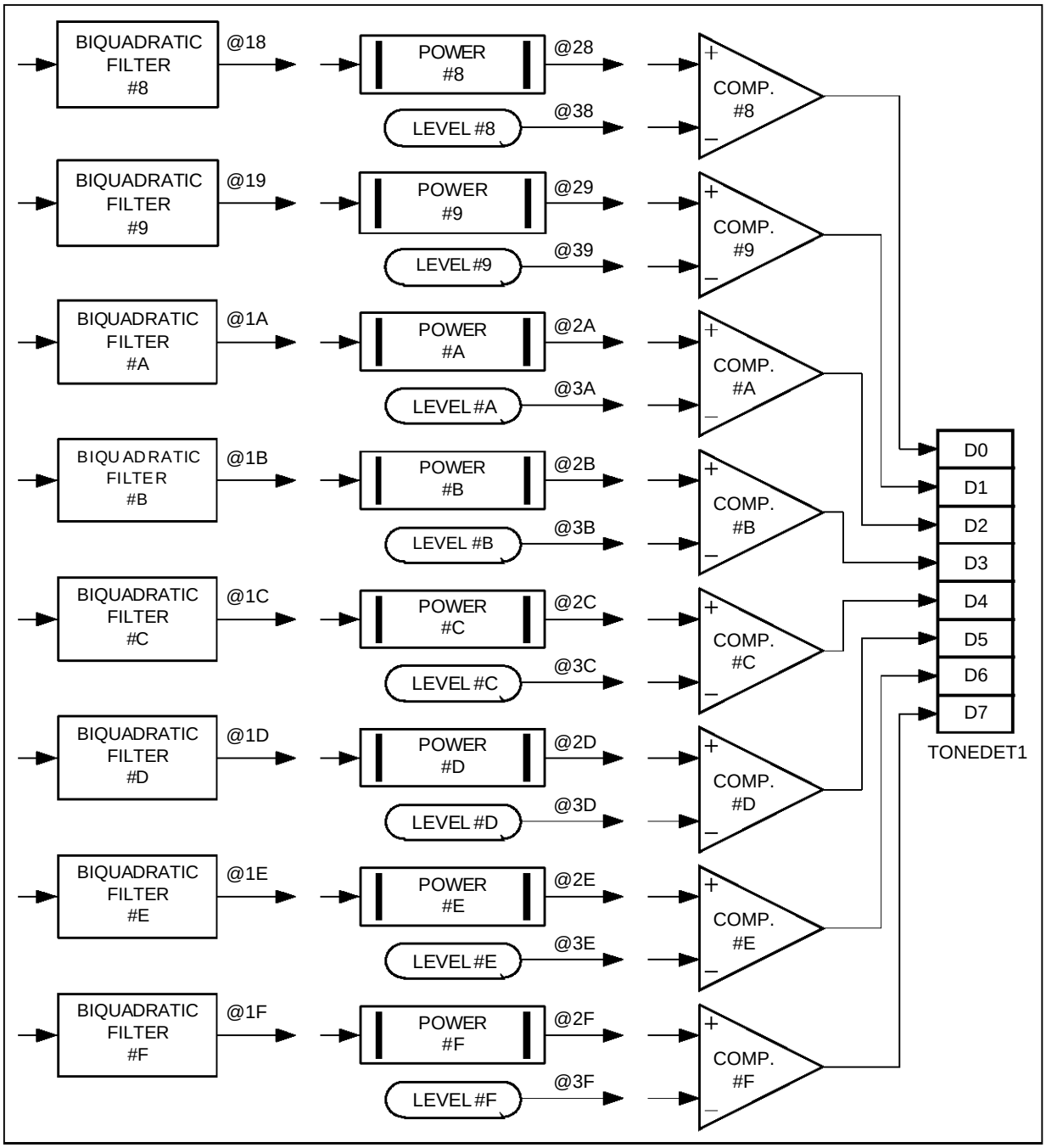


Figure 5 : Tone Detector Wiring Address (second half)

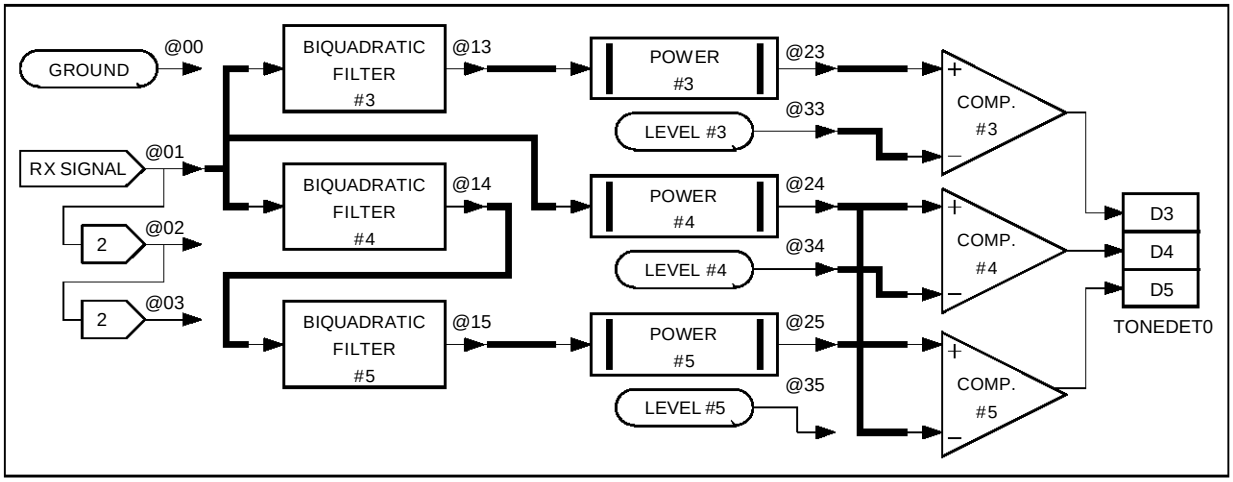


VIII.3 - Example

Hereunder is an example of programming a single Tone detection (using Cell #3) and a complex differential tone detection (using Cell #4 and #5).
Bit 3 of the TONEDET variable will be triggered each time the energy of that filtered signal is higher than Static Level number 3.

Bit 4 of the TONEDET variable will be on each time a receive signal has an energy higher than the Static Level number 4. Bit 5 will be on only when the Filtered (Filter section 4 and 5) received signal higher than the energy of the wide-band signal number 4 ; this prevents triggering on noise.

Figure 6 : Wiring Example



Program Cell #3 :

TDWW	**03**	**00**	**13**	**01**

Connect Received signal to Filter and Filter to Energy.

TDWW	**03**	**01**	**33**	**23**

Connect Level to Comparator Neg Input and Energy to Pos Input.

Program Cell #4 and #5 :

TDWW	**04**	**00**	**01**	**01**

Connect Received Signal to Filter and Energy.

TDWW	**04**	**01**	**34**	**24**

Connect Level to Comparator Neg Input and Energy to Pos Input.

TDWW	**05**	**00**	**15**	**14**

Connect Filter#4 Output to Filter and Filter to Energy.

TDWW	**05**	**01**	**24**	**25**

Connect Wide-band Energy to Neg Input and Energy to Pos Input.

IX - BUFFER OPERATIONS

IX.1 - Introduction

This appendix is dedicated to buffer operation, either the data buffers used in data exchanges or in particular Modes (like Voice).

The first part is oriented towards a functional description of the buffer operation, while the second section is more oriented towards the management of the buffers.

IX.2 - Receive Operations Overview

Figure 7 describes the receive data flow.

The ST75C52 can handle the following types of format for the data :

- parallel synchronous mode : 8-bit words are synchronously available in the receive buffers. The buffer status holds the number of valid bytes received,
- parallel HDLC framing mode : 8-bit data is available in the receive buffers. Framing information (like flags, CRC, additional "0") is interpreted by the ST75C52 and reported when necessary in the receive buffer status (CRC error, aborted frame, framing error, etc). This feature greatly eases the implementation of protocols as well as FAX data management.

Each time the receive deframer has filled up a new buffer, it sets the corresponding flag with the proper status then generates the IT3 interrupt. The availability of the buffers is tested just before starting to fill them. This further means that the host must not perform any buffer operation on the data part while the status remains 0.

IX.3 - Transmit Operations Overview

Figure 8 describes the transmit data flow. The following modes are available :

- parallel synchronous mode : 8-bit words are synchronously read from the transmit buffers. The transmit status buffer holds the number of valid bytes to be transmitted (up to 8 per buffer),
- parallel HDLC framing mode : 8-bit data is received from the transmit buffers. Framing information (frame open, frame close, frame abort, number of byte per buffer) is carried by the transmit buffer status and processed by the ST75C52. CRC, padding and other operations are automatically handled by the ST75C52.

Each time the transmit framer has emptied a buffer, the IT2 interrupt is raised.

Figure 7 : Rx Buffer Schematics

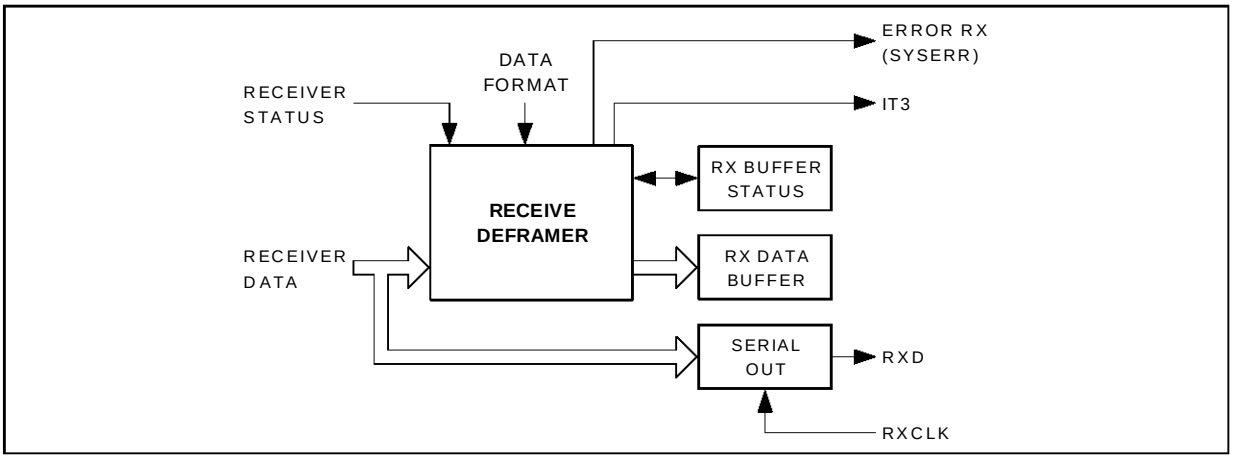
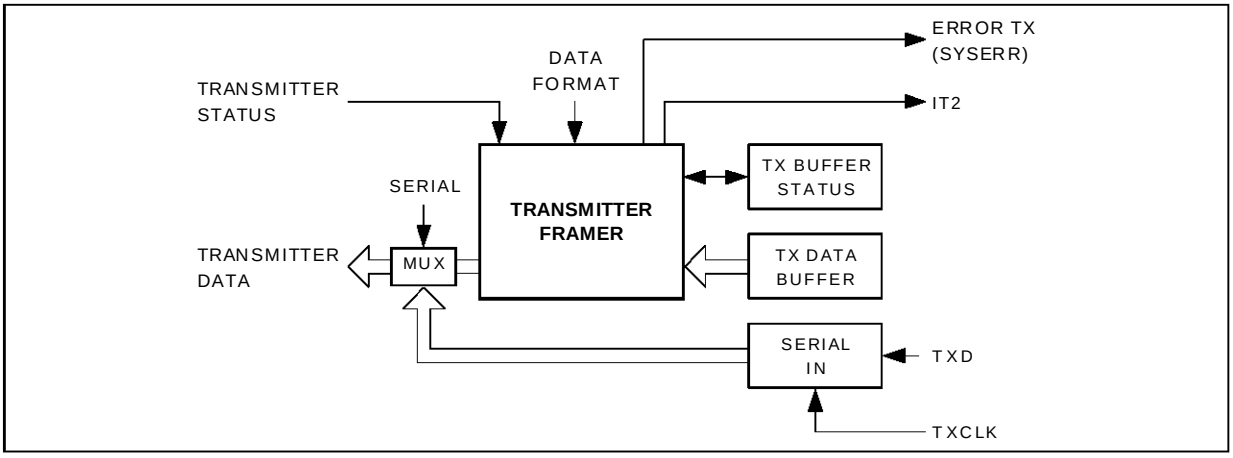


Figure 8 : Tx Buffer Schematics



IX.4 - Buffer Status and Format Description

The following section describes the meaning and use of the buffer status words.

IX.4.1 - Transmit Buffer

The transmit buffer status words are DTTBS0 and DTTBS1 (see the **Host Interface Summary** section in the main document) and are more likely to be seen as control words. These words must be set by the host and are reset by the ST75C52. The data buffer exchanges are synchronized through these status words, (see Buffer Status and format description) an improper setting will trigger the error Err_Tx in the error status SYSERR. A value of 0 for DTTBS0 or DTTBS1 means that the corresponding buffers are empty : this value is written by the ST75C52. The unused bits of DTTBSx must be set to 0 by the host.

In FSK Mode, when working in the parallel data mode, the transmitter expands each bit to the nominal baud time (1200Hz/300Hz/75Hz).

IX.4.2 - Synchronous Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer

IX.4.3 - HDLC Framing Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer
BUFF_SFRM	4	0 1	Data stream Start of frame
BUFF_EFRM	5	0 1	Data stream End of frame
BUFF_FRAB	6	0 1	Normal process Abort frame (no data in buffer)

IX.5 Receive Buffer

The receive buffer status words are DTRBS0 and DTRBS1 (see the **Host Interface Summary** section in the main document). These flags are set by the ST75C52 and must be reset by the host. The data buffer exchanges are synchronized through these status words, an improper resetting will trigger the error Err_Rx in the error status SYSERR. A value of 0 for DTRBS0 or DTRBS1 means that the corresponding buffers are empty : this value must be written by the host.

In FSK or V.21 Channel 2 Mode, when working in the parallel data mode, the receiver extract each bit using the nominal baud rate (1200Hz/300Hz/75Hz).

IX.5.1 - Synchronous Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer

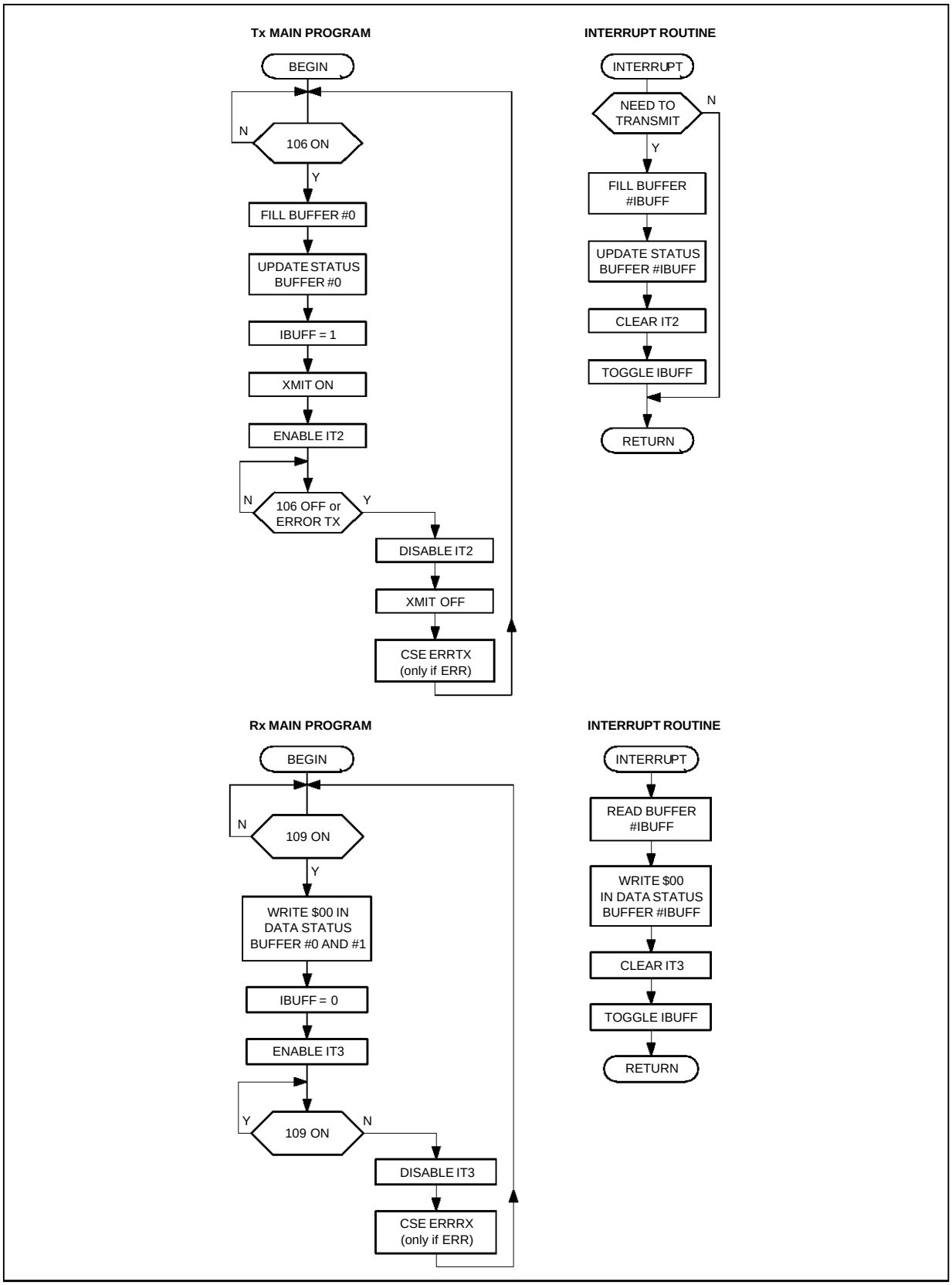
IX.5.2 - HDLC Framing Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer
BUFF_ERRS	5..4	00 01 10 11	No error CRC error Non byte-aligned frame Aborted frame
BUFF_SFRM	6	0 1	Data stream Start of frame
BUFF_EFRM	7	0 1	Data stream End of frame

IX.6 - Data Buffer Management

Figure 9 shows the general flow chart for transmit data buffer management. In the transmit path, the data buffer exchanges should always begin with the filling of buffer 0, then with the update of the buffer 0 status word. The initiation of the data exchanges is initiated then with the **XMIT** command.

Figure 9 : Buffer Operations Synchronization



75C52-27.EPS / 75C52-14.EPS

X - DEFAULT CALL PROGRESS TONE DETECTORS

Figure 10 : Call Progress Tone Detector Band 1

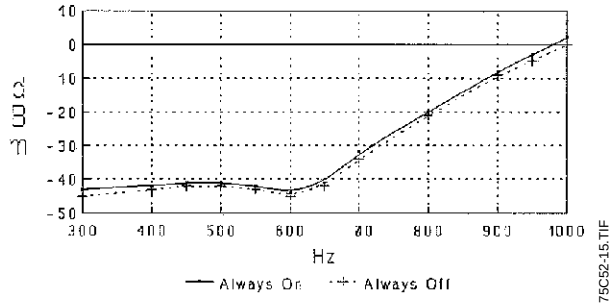
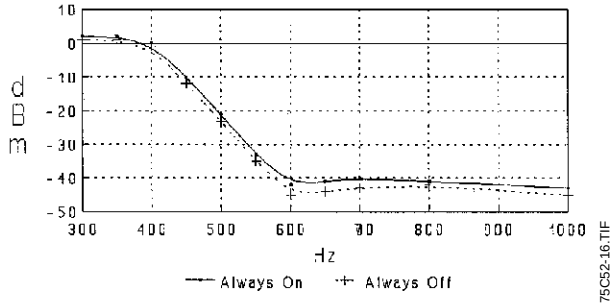


Figure 11 : Call Progress Tone Detector Band 2



XI - DEFAULT ANSWER TONE DETECTORS

Figure 12 : 2100Hz Answer Tone Detector

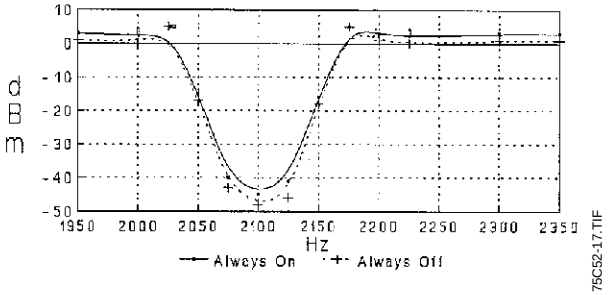
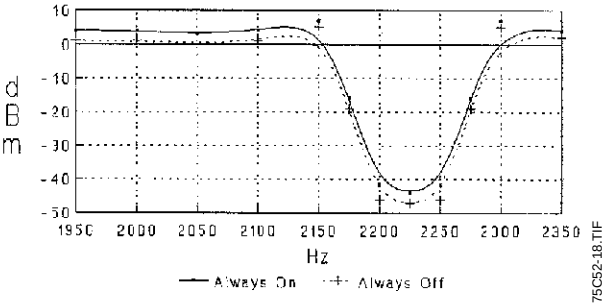


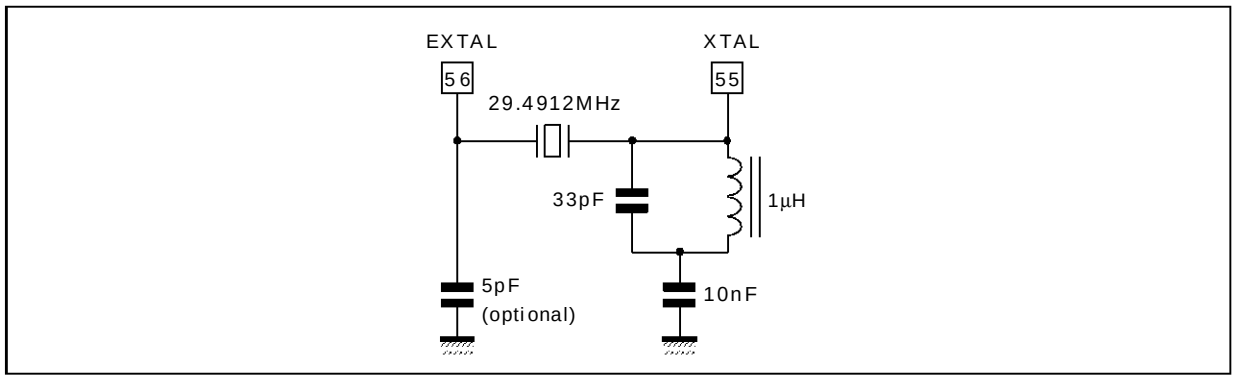
Figure 13 : 2225Hz Answer Tone Detector



XII - ELECTRICAL SCHEMATICS

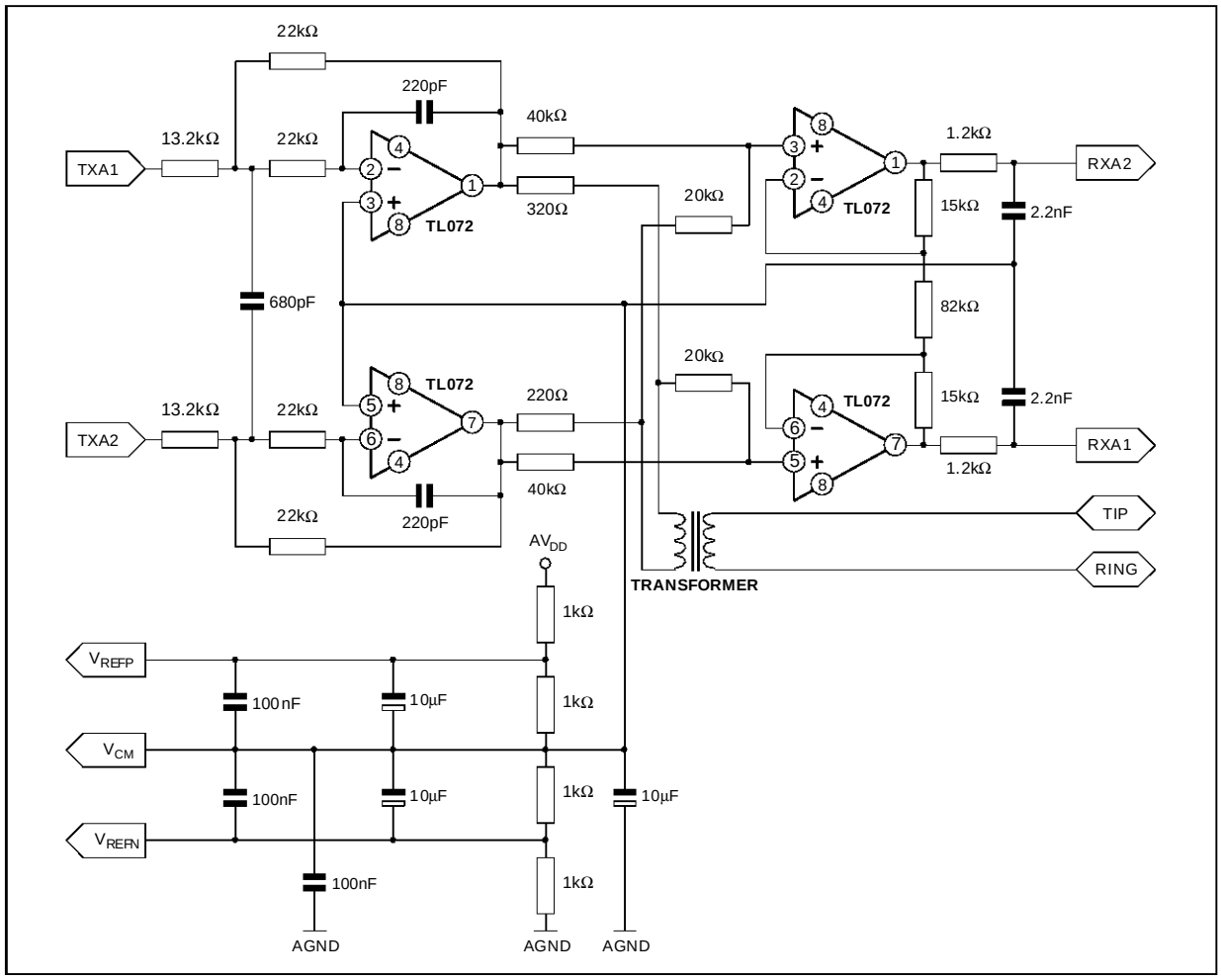
Oscillator

When using a third harmonic crystal oscillator in series resonance mode ($R_S < 40\Omega$, $C_0 = 6pF$, $P_e = 0.1mW$), we recommend the following schematic :



XII - ELECTRICAL SCHEMATICS (continued)

Figure 14



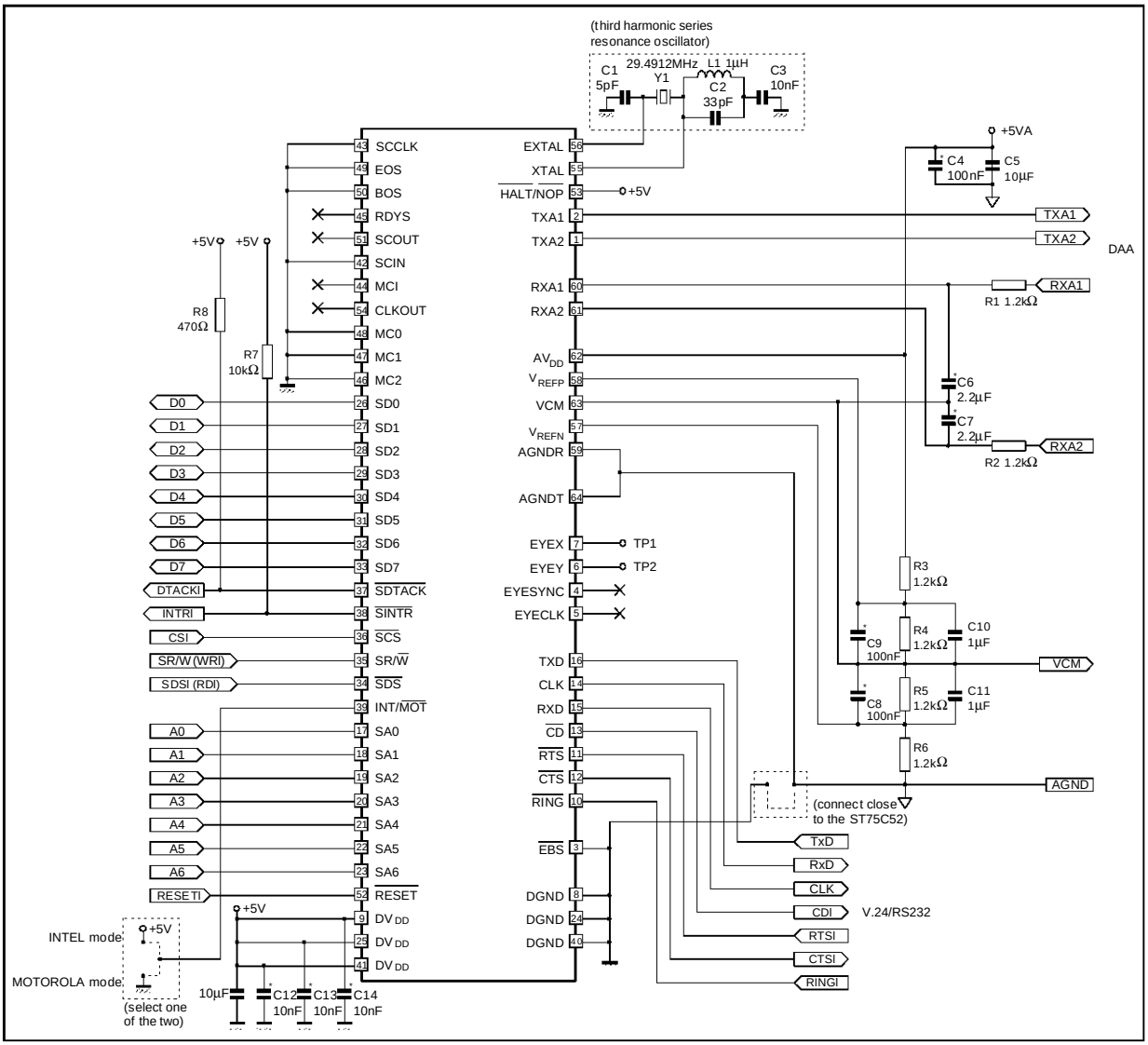
XIII - PCB DESIGN GUIDELINES

Performances of the FAX modem depends on the ST75C52 intrinsic performances and on the proper PC board layout. All aspects of the proper engineering practices, for PC board design, are beyond the scope of this paragraph.

We recommend the following points :

- in a 4-layer PC board :
  Separated digital ground and analog ground, connected together at one point, as close as possible to the ST75C52,
- in a 2-layer PC board :
  Provide a ground grid in all space around and under components on both sides of the band and connect to avoid small islands,
- both AGNDR and AGNDT must be connected with very low impedance to a single point, (see Chapter I.7, Power Supply),
- the two 2.2nF capacitors connected to the RXA1 and RXA2 Pins must be as close as possible to them,
- the two 100nF capacitors connected to the V_{REFP} and V_{REFN} pins must be as close as possible to them,
- analog and digital supplies must be connected together, at a single point, as close as possible to the chip (see Chapter I.7, Power Supply).

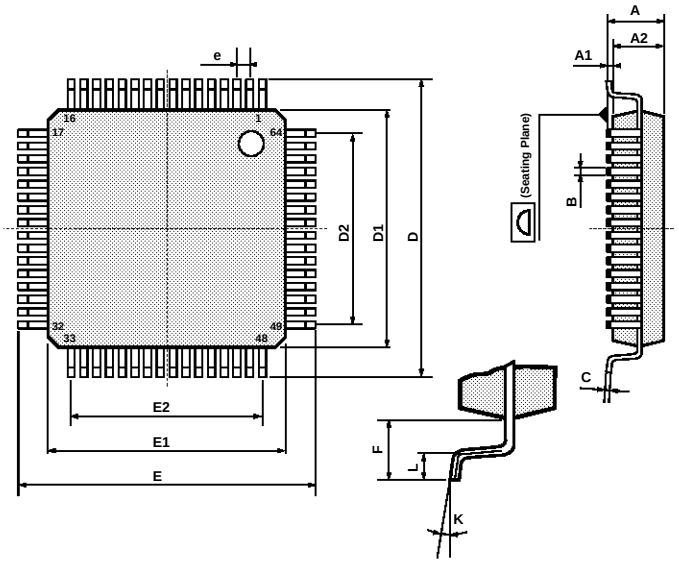
TYPICAL APPLICATION



Notes : All capacitor with a "*" must be implanted close to the ST75C52 pin.
All signal name ending with a "1" are active low.
R3, R4, R5, R6 are needed if the hybrid will sink a current on V_{CM}.

PACKAGE MECHANICAL DATA

64 PINS - PLASTIC QUAD FLAT PACK



PMPQFP64.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.10	0.11	0.12
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		12.00			0.472	
e		0.80			0.031	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		12.00			0.472	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.65	0.80	0.95	0.025	0.031	0.037

PQFP64.TBL